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Cascaded Converters For Integration And Management Of Grid Level Energy Storage Systems

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CASCADED CONVERTERS FOR INTEGRATION AND MANAGEMENT OF GRID LEVEL ENERGY STORAGE SYSTEMS

by

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Advisor Date

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DEDICATION

I dedicate my research work to Alaas family. A special feeling of completion of PhD degree to my dad and mom. Their words of support and encouragement still ring in my ears. Great thanks for my sisters, brothers and all Alaas family members who have never left my side. Also, many thanks to my uncles Zuhair, Abdullah and Ali. I will always appreciate all they have done. Finally, I dedicate this dissertation and give special thanks to my wonderful wife and my kids for being with me throughout the entire PhD program.

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CHAPTER 1 INTRODUCTION

Energy storage systems (ESSs) can help address many challenges in modern power systems, such as improving grid reliability, accommodating peak load demand, and increasing penetration level of renewable energy sources [1- 10]. Renewable energy such as wind and solar sources can reduce human's dependency on non-renewable energy resources. The former renewable energy sources, however, are intermittent in nature and could lead to power quality and system operation issues (i.e., voltage regulation, reactive power compensation, stability, and system reliability). Energy storage systems can be used to compensate for sudden changes in load demand and deficiency in power generation. They can also be used to store electrical energy during low demand, and give back the stored energy during high electricity demand. However, there are many types of ESS technologies, i.e., mechanical, electrical, chemical, thermal, electrochemical, and thermochemical. This research work is aimed at how to integrate large-scale electrochemical ESSs, i.e., Battery Energy Storage Systems (BESSs), to grid via new cascaded multilevel inverters.

The BESSs are one of the most important developments in the technology history. Today, some of the chemical and power industry sectors were established based on the discoveries of battery technologies. Large-scale BESSs provide numerous benefits, which allow them to be effectively utilized in different applications such as electric vehicles (EVs), intermittent energy sources and power utilities. According to the US Department of Energy (DOE), batteries are an essential component for battery based EVs [11]. Also, BESSs are more competent to have faster and better frequency response compared to other ESSs such as mechanical and thermal energy storage systems, which can be critical in situations of

sudden changes in system frequency. Fig. 1 illustrates the powerful of installing BESSs with a mechanical/thermal ESS, i.e., a hydrothermal plant like the one that is constructed in Chile [12]. In terms of frequency response, Fig. 1 shows two different cases, i.e., with and without BESS (case A: reserve provided by hydro and thermal power plants; and case B: reserve provided by BESSs, hydro, and thermal power plants). Both the cases represent the same volume, i.e., 400 MW. It is clear that the overall frequency response of hydrothermal power plant can be improved by adding battery energy storage system.

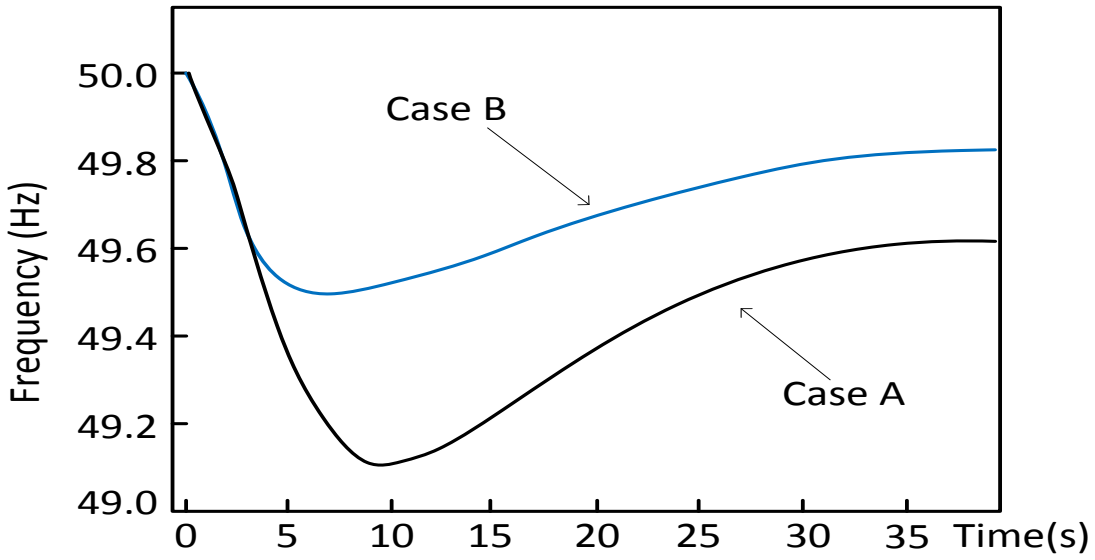


Fig. 1. Hydrothermal power system frequency response with/without BESS [12].

On the other hand, these technologies are facing many challenges. For example, in large-scale BESSs, battery cells/modules are connected in series and parallel for a desirable voltage and capacity level. Variations in production, age degradation, cell temperature and over-charge/discharge, however, affect the characteristics of battery modules/cells [13, 14]. This causes batteries to charge or discharge differently within the same chain. Battery modules/cells with lower energy capacity in the same string are more vulnerable to being over-charged or over-discharged while high energy-capacity batteries may be under-utilized.

For every cycle, the battery with the lowest capacity in the string will get weaker [15] and move closer to the point it will cause premature failure of the whole system [16]. Therefore, a uniform state of charge (SOC) operation is critical. Power electronic converter based battery management system (BMS) is a very important solution in addressing the above issue. In this chapter, problems statement, research purpose and literature review are given first. Then, a brief background of battery packs and cells are presented. Also, some important parameters that lead to increased interest in uniform SOC for large-scale BESSs are demonstrated. Finally, since the research work of the dissertation focuses on inverter topologies, the last part of this chapter covers the fundamental knowledge of multilevel inverter topologies and switching control.

1.1 Problem Statements

The SOC is an indicator of the available charge in a battery pack/module. For large-scale battery energy storage systems, balancing of SOC is important, which, in turn, protects weaker batteries while utilizing the available capacity of each battery module/cell in the whole system. Also, the output voltages of batteries are proportional to their SOCs. Hence, the imbalance of SOC among battery modules/cells in the same string will lead to produce output voltage steps with different amplitude in ac-side of cascaded multilevel inverters, which affects the Total Harmonic Distortions (THD%) of the ac output waveforms. In this dissertation work, different cascaded multi-level inverter topologies are developed and the corresponding battery management methods are devised to control individual battery modules/cells via the developed multi-level inverters to achieve and maintain a uniform SOC operation.

Due to modularity and scalability, traditional cascaded H-bridge multilevel (CHB) converter topology has been employed in many applications. However, the number of components used is large, particularly when the output voltage is high. New cascaded multilevel converter topologies are proposed to realize uniform SOC operation with fewer components compared to the traditional inverter. Regulation of power for continuous and uniform SOC management is carried out by controlling the modulation index of the switching devices of each battery module without adding additional balanced circuits. When one or more battery modules/cells have problems, and need to be bypassed for reconfigurable operations, it can be readily achieved by controlling the power electronic switching devices of the converters for these battery modules/cells. A phase-shifted pulse width modulation technique is developed for the both proposed inverters to control power of individual battery modules/cells. In this case, there is no need of carrier wave rotating process, which simplifies the drive circuits and further reduces the cost. The conduction times for the switching devices vary in the whole battery storage systems until when an equal utilization of battery modules/cells (or uniform SOC) is achieved.

1.2 Research Purpose

The objective of this dissertation is to develop new cascaded multilevel inverters to integrate and manage grid-level energy storage systems. Two different types of multilevel inverters will be developed. The first proposed inverter, called Six-Switch Cascaded Transformer (SSCT) multilevel converter, is different from the traditional cascaded inverters as the basic building block in the SSCT is a three-phase converter and each battery module will not be just interfaced to just one phase, but to all the three phases simultaneously. In

other words, the battery module will be the common dc-link for three-phase converters at the same position in a three-phase circuit. Traditional cascaded inverters suffer from issues of unbalanced loads among different dc sources. Certain unique differences between a SSCT inverter and a traditional inverter are listed as follows:

1) Sub-three-phase converters connected to the same battery will be controlled together as a core block in the system.

2) Modulation strategy for one battery converter is similar to others, making the control and gate drive circuits relatively simpler.

3) Three phase strings can be controlled together as a single three-phase inverter by using the d-q transformation technique.

4) Highly reliable operation.

The second proposed inverter is a Hierarchical Cascaded Multi-level Converter (HCMC). Its hybrid design comprises of a half-bridge (SOC is achieved at the half-bridge level) converter and an H-bridge inverter through which the voltage is passed to reach a high-level. The system can handle heterogeneous batteries. Nevertheless, in HCMC, batteries with same specification can be grouped as a sub-system within the large-scale system, which makes monitor and control relatively easier. Due to the battery capacity differences in the three phases, they can have different SOC values. Hence, a new three-phase SOC equalizing circuit, called Six-Switch Balancing Circuit (SSBC) is proposed to realize uniform SOC operation for full utilization of the battery module/cell in the three-phase BESS while keeping balanced three-phase operation. Moreover, in the hierarchal

structure, the required number of switching devices is reduced compared to traditional CHB inverters.

1.3 Literature Review

In the last few decades, several multilevel inverter structures have been suggested for realizing high output voltage and power. Multi-level inverters, designed to generate low-cost power, are used in grid-connection applications at different levels of voltage (medium and high voltage levels) because in most cases it is hard to connect a single power semiconductor switch directly to the gird [17]. Such technologies also reduce total harmonic distortion (THD %), dv/dt, and electromagnetic interference [17-73]. Multi-level inverter topologies can be grouped into common dc-link [17-26], cascaded separate dc sources [17, 74], isolated topologies [29-47], and interconnected three-phase inverters [48]. In addition, other types of topologies have also emerged such as the one implemented by means of cascading basic cell structures called hybrid inverters. However, some of those topologies combine more than one fundamental converters or conventional cascaded multi-level structure [49-73].

Common dc-link multilevel converters, such as diode-clamped or Neutral Point Clamped (NPC) converter, capacitor-clamped or Flying Capacitor (FC) inverter, and Modular Multilevel converter (MMC), were proposed for high power applications. In an NPC inverter, capacitors are connected in series to share the voltage where diodes are used to clamp voltages across capacitors. As a result, each switch stands only with one capacitor voltage [48]. However, the inverter suffers from capacitor unbalance voltage issue and unfavorably big number of clamping diodes when the number of voltage level is large [22].

Reverse recovery of clamping diodes is another design flaw when the inverter is controlled under Pulse-Width Modulation (PWM) techniques [17]. Capacitors, in a flying inverter, are employed to clamp voltage across switches. It is similar to a diode-clamped inverter but with more capacitors. Moreover, this type of inverter needs complicated control strategies to regulate the floating capacitor voltages [48]. However, the MMC topology is a common dc-link but with a cascaded multilevel structure where the converter is characterized by a modular arm with upper/lower legs composed of series connection of power converter modules [75]. The advantages of high modularity and voltage scalability allow this structure to be connected directly to grid with no need of transformer. Capacitor voltage balancing is simpler compared to other common dc-link multi-level converters, which makes the modular multi-level converter useful in many applications. Large inductors are a must for an MMC converter to regulate the flow of current due to the varying voltage over the arm inductor. Another issue is the quantity of capacitors [25, 75]. However, all battery modules/cells in the previous common dc-link multilevel converters have a common dc link where all system battery packs are connected in series and parallel, thereby sharing the total power. Such converter topologies are not desirable for large-scale energy storage systems when we need power management on each individual battery module/cell.

Cascaded H-bridge (CHB) multi-level inverters do not require clamping diodes or capacitors [17]. They are energy efficient, and their design is based on a modular structure. The technology has been used in variable-speed drive (VSD), static Var compensation (SVC) and other flexible AC transmission system (FACTS) applications. CHB inverters have low voltage single-phase H-bridge modules and a separate dc source for each cell-

module. For every separate dc supply, the control has to be performed at each phase; a more complicated task than in a *dq* frame for three phases. Pulsating power is another issue.

In some certain application areas such as in EVs, only one battery pack is desirable [46]. Also, an isolated system of battery charger is preferable, which can be realized by using transformers operated at high frequency to reduce size and cost [47]. For these reasons and more, new families of isolated multilevel inverter topologies have been proposed [32, 33, 35]. Moreover, those isolated inverter topologies provide a filtering effect of harmonic components due to leakage reactance of cascaded transformers [33]. To elevate the output voltage of isolated converters, cascaded transformers are used instead of cascading separate dc voltage sources. Cascaded transformer multilevel topologies are different from traditional H-bridge cascaded inverters where each dc source or basic cell is not just interfaced to just one phase, but to all three phases. In other words, each basic cell will be the common source for a three-phase converter at the same position in a three-phase circuit. Control strategies for these basic cells are different as well. Traditional cascaded inverters experience issues of unbalanced loads among different battery strings of three-phase BESS systems [24]. In an isolated inverter structure, each basic cell can be loaded equally in principle because the basic cell will be controlled as a core block in the system; and hence, the modulation strategy for all dc sources are similar to others, making the control and gate drive circuits relatively simple. The three-phase strings can be controlled together as a single three-phase inverter by using the d-q transformation technique.

Hexagram multilevel converter, which belongs to the family of interconnected three-phase converter, comprises of six three-phase converter modules [82]. Energy efficiency

coupled with a built-in fault tolerance mechanism makes Hexagram converters more desirable in applications where CHBs are used. The converter, however, must have a large inductor to regulate the flow of current. The limited number of steps in the voltage waveform may result in a larger value of THD [48]. Another disadvantage is that modules equally and automatically share the total power which makes Hexagram and other interconnected three-phase converters not-so suitable choice for large-scale battery energy storage systems where different battery modules may carry different power for SOC management purpose.

In general, the CHB multilevel topologies can be categorized into symmetric or asymmetric structure [74]. For both types of inverter, there are isolated dc supplies. But the values of separate dc sources are different in asymmetric converters. For the same number of output steps, the essential requirement for more separate dc sources may be viewed as a drawback of symmetric CHB inverters. However, this feature can be considered a solution for certain applications (e.g., large-scale BESS systems) due to the modularity structure of using identical/similar power cells [74], simplicity of control [56], and hence, an effective way to reduce cost [74]. A major requirement, however, for power switching devices is the main challenge of symmetric CHB in high voltage and power applications. As a result, in practical implementation and high voltage-level requirement, reducing the number of semiconductor devices and gate-drive circuits are strongly desirable, without losing modularity of the inverter structure. Numerous hybrid structure topologies have been presented in [49- 73] to address component requirement issues. One of those new family structures uses a hybrid combination of single H-bridge converters and cascaded basic cells [49- 58]. The H-bridge inverter generates polarity of the output voltage. Three different

topologies of 11-level multilevel inverters have been suggested in [49] that use a diode clamped leg, capacitor leg or cascaded basic cell of two switches to control power of each dc source. In addition, asymmetrical single-phase multilevel topology was described in [50]. DC sources can be identical but not isolated from each other. Moreover, each dc supply needs three switches on the top of using an H-bridge inverter. In [53], a new switched-capacitor inverter was proposed, which is easier to implement when compared to a conventional SC inverter, and comprises of a Marx converter building structure and an H-bridge. It only needs one dc source but more capacitors are needed as the voltage level requirements increase. Recently, a 41-level inverter has been suggested in [56], which uses only 14 switching devices to perform both positive and negative output voltages. In this inverter, all dc sources are connected in series, and hence converter cannot isolate an individual battery modules or cells. In the afore-mentioned topologies (i.e. [49- 58]), however, the number of voltage-levels and cascaded basic cells is limited to an extent by rated values of both dc sources and single-phase H-bridge converters.

To address some of the aforementioned challenges, several new cascaded *m*-level multilevel converters have been proposed in [59- 61] to elevate the output voltage level. These new inverter topologies consist of hybrid sub-multilevel blocks. Circuits of these blocks are cascaded through m-level multilevel converter cells to meet the output voltage requirement with higher voltage level steps compared to cascaded multilevel H-bridge inverters. In [59] a phase-disposition level-shifted PWM technique has been proposed to implement a hybrid multi-cell converter. However, this topology employs a Fly Capacitor (FC) converter, which generates a positive voltage steps and hence form a variable dc-link

voltage. Due to the use of capacitors in the basic FC cell, this topology is not recommended for large scale BESS. Additionally, in [60], another topology of FC converters was presented but with two converter legs. The first leg is a flying capacitor inverter with a certain voltage-level while the second leg is a half-bridge to connect or bypass the basic cell. This topology faces the same challenge of the previous topology and it has an asymmetric structure. In [61], the authors proposed two cascaded m-level multilevel inverters. In both topologies, the basic cell has two legs of common dc source converters and those legs may be diode or capacitor clamped inverters. As a result, these types of inverter structures have the same drawback of the traditional common dc source inverters. More other types of inverter topology can be found in [62-73].

In this dissertation work, two new-cascaded multilevel inverter topologies are presented to integrate and manage grid-level battery energy storage systems. One of the developed converters, the Six-Switch Cascaded Transformer (SSCT) multilevel converter, is different from the traditional isolated cascaded H-bridge multilevel inverter, which has only one battery packs string. The second proposed multilevel inverter is a hierarchical-cascaded multi-level inverter with the ability to achieve uniform state of charge operation and transfer power between battery strings (phases) of the three-phase BESS system.

1.4 Battery Pack/module

Battery pack or module can be designed from multi-chemical cells to provide a wide range of integrated power sources. In other words, battery packs are built up from series and parallel strings of low voltage and low capacity cells. In case of a pack made from only one series chain and identical cells, the pack capacity in Amp-hours has the same capacity of

single individual chemical cell since all the cells have the same current but the battery pack achieve a higher voltage and certain Watt-hour capacity. To increase the pack capacity, more parallel connections of cell strings are needed, and hence the Amp-hour and Watt-hour capacities are increased. The rated voltage of a single cell is determined by the chemical materials used in cell production. The following section demonstrates some of the different battery technologies that can be used in large-scale battery energy storage systems.

1.4.1 Electrochemical Battery Technologies

Battery technologies, dubbed as one of the oldest energy storage systems, store electrical charge by converting it to chemical energy. All electrochemical ESS technologies are used in a format of rechargeable electrochemical sources. Some of electrochemical energy storage system technologies are shown in Fig. 2 [9]. As illustrated in Fig. 2, an electrochemical ESS comprises at least one electrochemical material, which contains positive and negative electrodes with a solid or liquid electrolyte.

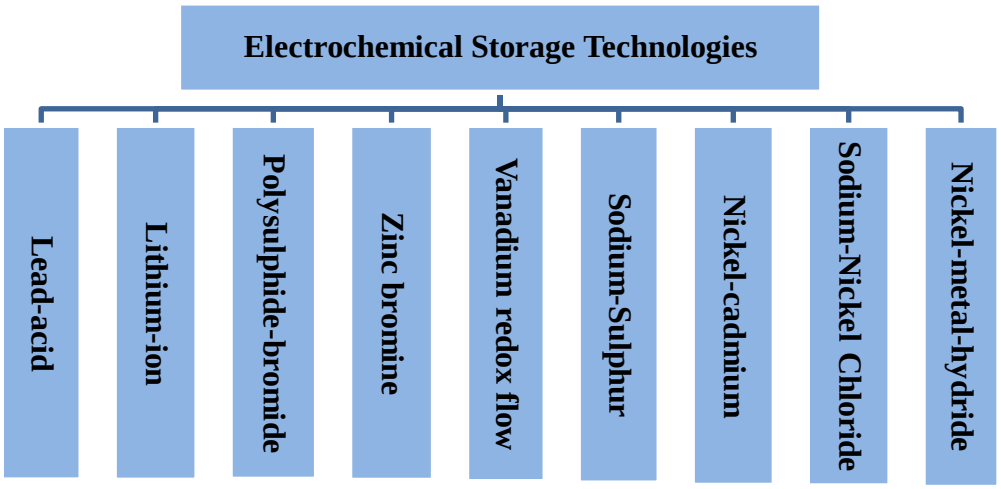


Fig. 2. Electrochemical energy storage system technologies [9].

Nowadays and overall electrochemical technologies, the commercial-scale batteries used in power industry are Lead-acid, Lithium-ion, Sodium-sulphur, Vanadium redox flow,

and Nickel-metal-hydride [76]. These batteries are capable to be used in large-scale BESSs and EVs. Table 1 summarizes the major features for each of these electrochemical technologies which have different cell chemistry output voltage, sizes and various characteristics.

Table 1 Comparisons of various types of battery technologies [76, 77].

Type	Lead-acid	Sodium sulphur	Redox flow	Nickel metal hydride	Lithium-ion		
					$LiCoO_2$	$LiMn_2O_4$	Li-Metal
Commercialization	Mid-1800s	1960s	1970s	1990	1992	1999	2003
Cycle life (100% DOD)	200-1,000	2,500-4,000	>12,000	180-2,000	1,000-10,000		
Round trip efficiency	75-85	75-90	75-90	~ 65	85-97		
Self-discharge	low	-	negligible	high	medium		
Cell voltage (V)	2.0	2.1	1.5-1.55	1.2	3.7	3.6	4
Capital cost (US$/kWh)	100-300	300-500	150-1,000	900-3,500	300-2,500		
Energy density (Wh/kg)	25-50	150-240	10-30	60-120	75-200		
Power density (W/kg)	75-300	150-230	80-150	250-1,00	500-2,000		

Lead-acid battery was developed more than a century ago and has been widely used in battery storage systems. It is divided into two categories: flooded and sealed batteries. The lead-acid contains a lead dioxide (PbO_2), sponge lead (Pb), and sulfuric acid ($H2SO_4$) which, are used as positive, negative electrodes, and electrolytes respectively [2]. The flooded technology is the less expensive compared to sealed battery but requires frequent maintenance to check distilled water level. Also, flooded batteries produce flammable gases. The sealed battery uses a valve to reduce water loss which leads to a lower maintenance. As shown in Table 1, the main drawbacks of lead-acid technologies are low cycle life and low energy density. On the other hand, these batteries are still primarily employed in applications

where cost effectiveness and reliability are critical but energy density and cycle life are not as important. Nevertheless, a new technology called ultra-battery which is an advanced lead-acid battery. This technology is synthesized by introducing negative electrode of ultra-capacitor into the traditional lead-acid battery which improves the performance of lead-acid technologies [76].

A Nickel-metal- hydride (NiMH) battery storage is a type of Nickel-cadmium technology. The Nickel-cadmium battery is an electrochemical storage device that consists of nickel hydroxide and cadmium as electrodes and the positive and negative electrodes are detached by separator. In Nickel-cadmium technology, the electrolyte is an alkaline electrolyte. Compared to other Nickel-cadmium batteries, the NiMH batteries have higher power and energy density. However, NiMH technology suffers from high self-discharge rate, limited lifetime, and low Coulombic (round-trip) efficiency as shown in Table 1. As a relatively smaller scale rechargeable battery, the NiMH batteries have been applied for EVs and hybrid EVs in the 1990s and 2000s [76]. Moreover, NiMH battery packs were adopted for plug-in EVs such as General Motor's EV1, Honda's EV Plus, and Ford's Ranger EV. Also, these technologies are emerged in hybrid EVs (e.g., Toyota Prius, and Chevrolet Malibu hybrids) [76].

One of the solid-state technologies is a Sodium-sulphur (NaS) battery [2]. It is a type of molten-salt batteries, which are constructed from sulphur and sodium liquid electrodes. A sodium polysulphide is shaped when sodium ions (Na^+) are passing through the electrolyte and combines with sulphur. In discharging process, the Na^+ move from side to side of the electrolyte while the electrons move through the external circuit. The process is reversed

during charge operation [9]. The NaS technologies have been gradually grown since 2002 to be used in large-scale BESS for electric grid applications [76]. These batteries provide high energy density, i.e., 150-240 Wh/kg, and long cycle life but the power density is relatively lower compare to NiMH and Lithium-ion batteries as shown in Table 1. The NaS battery has the ability to work at high temperatures. Due to these advantages, in stationary BESSs, the NaS technology played a significant part in supporting power system (i.e., utility energy storage, load leveling, emergency power supply, and UPS applications). Over the last decade, power generation from wind farms and solar plants were supported by NaS battery. For example, in Texas, the world's largest NaS battery station (i.e., 4-MW) was built in Presidio since 2010 [76].

Redox flow batteries have been developed, such as Vanadium redox batteries, zinc-bromine, and polysulphide-bromine. The zinc-bromine electrochemical energy storage technologies have two separate tanks, containing different liquids which are zinc and bromine solutions, are used to store energy. During charge process, zinc is set down at the negative electrode and bromine is produced at the positive electrode. During discharging process, zinc and bromide ions are formed and combined to shape zinc-bromide with 1.8V across each cell [2]. To store energy, the vanadium redox battery employs two tanks of analytic and catalytic reservoirs containing Sulphuric acid solution [2,9]. The positive ions (H^+) are transferred between storage tanks during charging and discharging operations [4]. In Polysulphide-bromide battery system, the process involves a reversible electrochemical reaction between two salt-based electrolytes, sodium bromide and sodium polysulphide [2]. Polymer is used as a separator between electrolytes, which only allow the pass of positive

sodium ions. Among redox flow technologies, the vanadium redox battery is more favorable because the vanadium is employed as both positive and negative electrolytes. As a result, electrolytes can be remixed to recover capacity decay due to active ions transfer. Also, these technologies generate less hydrogen, because the potential of redox at the negative electrode is higher than the potential of hydrogen evolution [76].

In charging process, Lithium-ions, transferred by the potential difference supplied by the charging unit, intercalate into the inter-layer region of an anode (the most commonly used active material for anode is graphite). During the initial activation process, the movement of positive Lithium-ions in graphite is coordinated by the surface-electrolyte-interface layer. Also during the charging process, the Li^+ moves through the electrolyte and finally arrives at the anode while the oxidation state of the host metal will increase which lead to return electrons to the outside circuitry and vice versa the process is reversed in discharge process [76]. As shown in Table 1, Lithium-ion battery technologies have high power densities (due to the advantage of high cell voltage), high charge/discharge efficiency, long cycle life with deep discharge, and environmental friendliness.

However, electrochemical storage technologies improvement is basically boosted by demand for smart grid and EV applications. The Sodium Sulphur was the leading choice in the electric power sector until 2014 [76]. Nevertheless, as shown in Fig. 3, this preference choice slowly switched to favor lithium-ion and redox flow technologies. This is due to the performance enhancements and cost reductions realized by these storage technologies. The installed lithium-ion capacity is planned to increase quickly, and lithium-ion technologies have become the dominant storage technology for the future battery energy storage systems.

Also, lithium-ion technologies are gaining more interest in EV applications [76]. Tesla and AES are popular battery vendors. These big companies pick lithium-ion storage technologies as their battery products which lead to high competition in future ESSs market. The redox flow technology also displays cumulative attention in large-scale BESSs [76].

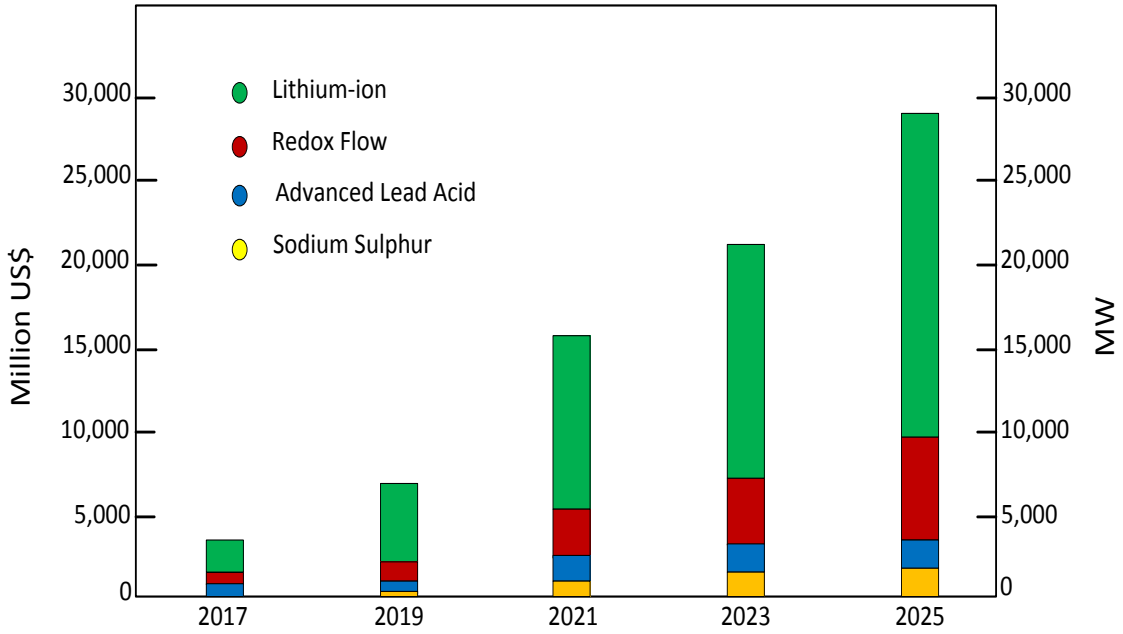


Fig. 3. Commissions (MW) in the worldwide power sector [76].

1.4.2 Battery Management System

Any power electronic system that manages rechargeable battery modules/cells or battery packs by controlling the charging and discharging processes, cell balancing, temperature, prediction of health-level and protecting the battery strings from operating outside the safe operating area is known as battery management system (BMS). Therefore, an effective and reliable BMS is a key module for a battery storage system even with significant progress in storage chemistries and materials. The main functions of the BMS include the gathering of date measurements of current, voltage, temperature and other parameters. Hence, ensure high accuracy estimation to protect battery cells/modules from

over-charge/discharge, and over-heating while increasing system utilization, prolong of cycle life, and reduce degradation of energy/power density. As a matter of fact, internal states of pack cells/modules are basically inaccessible. To overcome this problem, modeling of battery is developed to imitate and match module dynamics with a real electrochemical storage module.

1.4.2.1 Battery Modeling

Large-scale BESS systems consist of a huge number of battery packs in series/parallel connections to satisfy system output requirements. For these thousands of battery cells, a key task to develop effective battery management functions is battery modeling. To study the behavior of electrochemical storage module, many different models have been developed, such as electrochemical [78], stochastic [79], black-box [80], and electric equivalent network battery modules [81]. The electrochemical modeling approach is preferred by battery manufactures and chemistry researchers [78]. The stochastic scheme approximates internal states by process of discrete-time transient stochastic. The black-box modeling is a mathematical representation that battery is modeled by using fuzzy logic or artificial neural networks. However, power and electric engineers prefer to use the equivalent network model to express battery in terms of electric quantities such as voltage, current, and internal impedance. Fig. 4 displays a general equivalent circuit of rechargeable battery module where E and E_p are the main cell and parasitic reaction electromotive forces respectively. Both electromotive forces are the function of cell SOC and inner cell temperature T with the assumption that T is uniform. The parasitic reactions are not related to charge buildup inside the battery cell. In some electrochemical storage technology,

parasitic reactions are created by the water electrolysis that takes place at the end of the charging process [82]. The behaviors of internal dynamics of each induvial battery modules are affected by their SOCs as shown in Fig. 4.

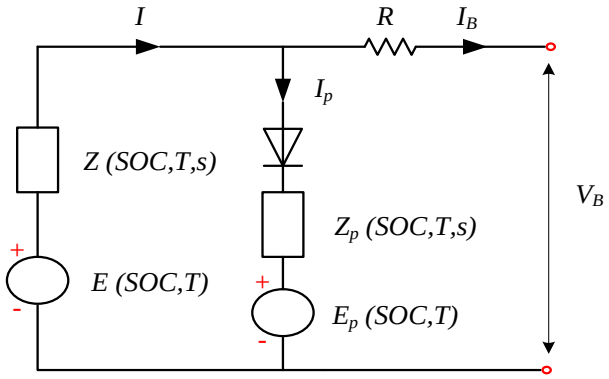
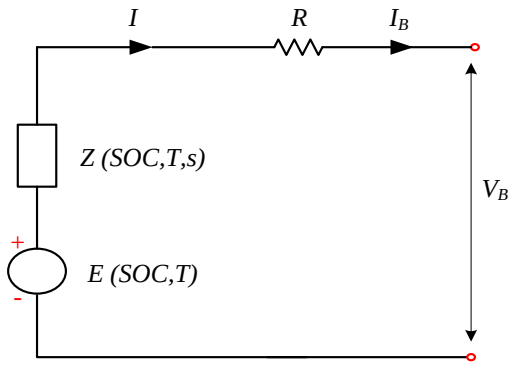
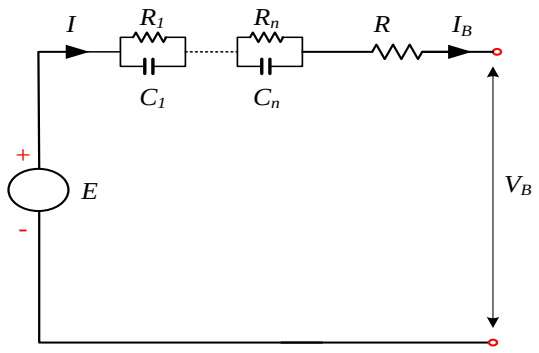


Fig. 4. Equivalent circuit of rechargeable battery model (discharging process) [82].

However, lithium-ion battery cells have high coulombic efficiency (round trip efficiency) and hence parasitic reaction effects are negligible [82]. As a result, the battery module of lithium-ion cells can be simplified as shown in Fig. 5 (a). The impedance Z is represented in Laplace domain s which also a function of cell SOC and T. Moreover, both output cell voltage V_B, and cell current I_B are dependent on R (cell internal resistance). In this case, the battery module can be as shown in Fig. 5 (b) where the number of RC blocks most often is in a range from zero to three [83].



(a)



(b)

Fig. 5. Equivalent circuit of rechargeable battery model: (a) A simplified battery module (without parasitic reactions), (b) *R-C* network for battery cell with high coulombic efficiency [83].

1.4.2.2 SOC/SOH States

Without suitable battery management, disastrous hazards may occur which lead to unpredicted failures such as short circuit, and uncontrolled thermal operations. To avoid such undesirable system operations, information of State of Charge (SOC) and State of Health (SOH) are crucial for battery energy system. In general, the SOC is defined as the energy left in a battery cell/ module compared with the energy of full battery cell/module as shown below:

$$\text{SOC} = \frac{Available\ capacity\ (Ah)}{Rated\ capacity\ (Ah)} \times 100\% \qquad (1.1)$$

The SOC gives an indication of how much longer the cell/module will continue to perform before it needs recharging. However, The SOH reflects the general state of a battery cell/module and its ability to deliver the specified performance compared with a new battery cell/module. Therefore, SOH takes into account some factors such as charge acceptance, internal resistance, voltage, and self-discharges that can be used to indicate battery lifetime and how much capacity left before cell/module must be replaced. In other words, the SOC is used to measure the short-term capability of the electrochemical storage while the SOH is

the measurement of long-term condition and both states affect each other. Fig. 6 shows the coulombic efficiency loss due to the hysteresis effect in a lithium-ion battery cell. In the graph, both *A* and *B* areas represent the over-charge/discharge regions, respectively. Battery module/cell should be not operating in these regions to prevent high charge/discharge stresses which lead to reduce lifetime. Therefore, it is critical to keep all battery modules/cells work within the safety range to avoid excessive over-charge/discharge and thermal runaway.

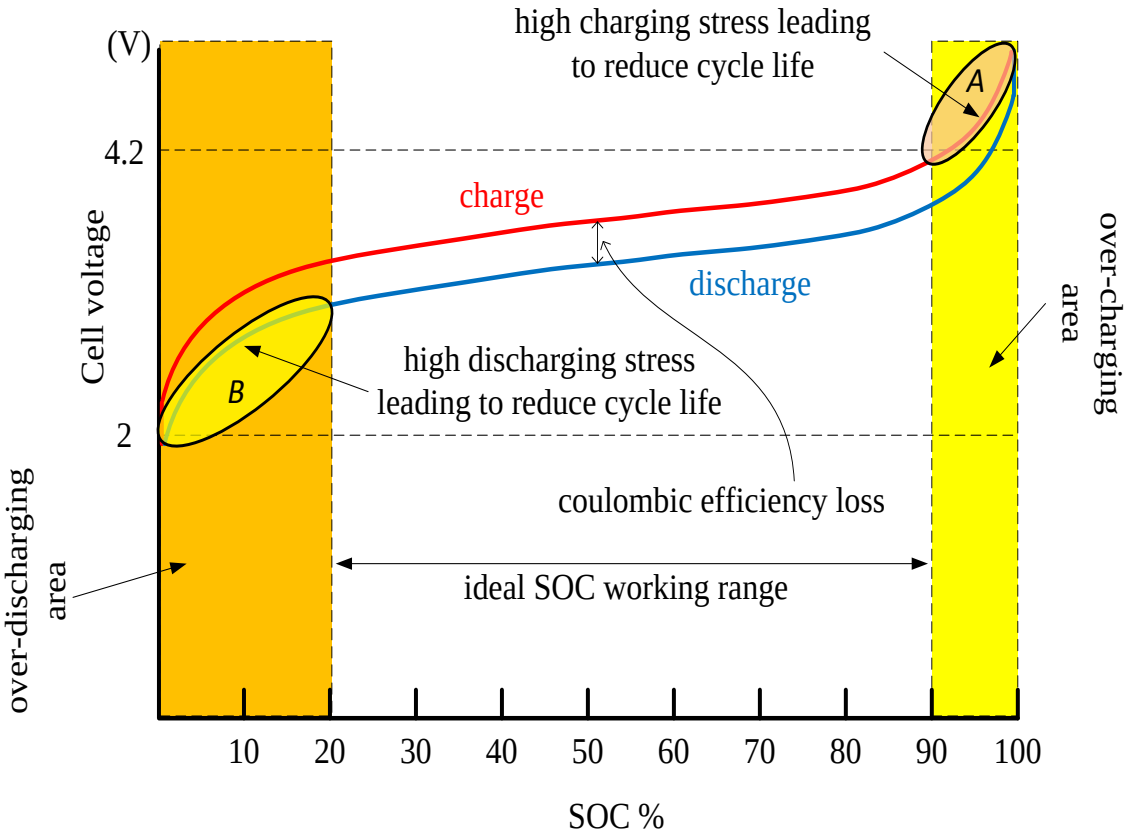


Fig. 6. The charge/discharge curve in a Lithium-ion battery cell [84].

One of the most challenges when dealing with large-scale battery energy storage systems is the measuring of available energy in each battery cell, i.e., SOC and remaining lifetime due to the state of battery aging (SOH). However, none of these parameters is

directly measurable by using sensors, leading to the need of estimation methods. For SOH, the battery is considered to reach its end of life when the module/cell capacity drops to 80% compared to the capacity of new module/cell [85]. This research work focuses on balancing SOC by using topologies of cascaded multilevel inverters based battery management system. Hence, for SOC estimation, the methods are classified according to estimation methodology as shown in Table 2. However, since the aim of this dissertation work is not intended for the accuracy of SOC estimations, the implementation of the prototype circuit in Chapter three is based on the terminal voltage estimation method. The electromotive force *E* in Fig. 5 is proportional to the battery terminal voltage. Moreover, *E* is approximately proportional to the SOC [86]. As a result, the terminal voltage of battery module/cell is also approximately linear proportional to SOC. But the estimation error becomes large at the end of discharge process because the terminal voltage suddenly drops as shown in Fig. 6.

1.4.2.3 Cell Balancing

Usually, a battery pack or module composed of a string of electrochemical cells. These cells are all the same type of chemistry materials and specification, but cell variances are occurring that increase with battery pack/module usage. To overcome this drawback effect, balancing of SOC, and voltage are desirable. Several cell balancing schemes have been proposed such as passive and active technologies [76]. The extra charge of higher capacity cells are consumed by the passive technique through external circuits (through bypass resistors). In the active technique, the energy moved from higher capacity cells to another low capacity cells. (for example, through capacitors).

Table 2 Example of SOC estimating methods [86].

Categories	Example of Estimation Methodologies
Direct measurement	Open circuit voltage
	Terminal voltage
	Impedance
Book-keeping estimation	Coulomb counting/Modified method
Adaptive systems	Kalman filter
	Fuzzy neural network
	RBF neural network
	BF neural network
	Support vector machine
Hybrid	Coulomb counting with Kalman filter
	Coulomb counting and EMF combination
	Per-unit system with EKF

Furthermore, for a battery pack or module, its battery management system performs a significant task in estimating pack/module SOC, which is known as "fuel gauge". In large-scale BESSs, battery packs/modules are connected in series and parallel for a desirable voltage and capacity level. Battery packs/modules face the same challenges of single cell, i.e., variations in production, age degradation, high cell temperature and over-charge/discharge, that cause battery packs/modules to charge or discharge differently within the same chain. Battery packs with lower energy capacity at risk to be over-charged or over-discharged while healthy batteries may be less utilized. For every cycle, the risk is increased, and weak batteries move closer to the point it will cause premature failure of the whole system. Power electronic converter based battery management system is important in addressing this issue. Multilevel inverters have been proposed for BESSs including the battery systems in EVs and grid-connected battery energy storage systems [87-124]. The

following section gives some background of the traditional multilevel inverters and basic converters that are used in the proposed topologies.

1.5 Power Converters

In the 1980s, the development of medium-voltage drives and high power electronic inverter topologies started and hence 4,500V Gate Turn Off GTO thyristors came to be commercially available [125]. On the other hand, before the 2000s, the GTO stayed as the typical switching device for the MV drive until new two semiconductor devices appear, i.e., Insulated Gate Bipolar Transistors IGBTs and Gate-Commutated Thyristors GCTs [126, 127]. The GTOs are replaced by IGBTs and GCTs due to the superior features of these new devices such as snubber-less operation, switching characteristics, reduced power consumption in power devices and simple control and hence rapidly used in many applications especially in main areas of high voltage and power applications. This section introduces basic converter blocks that are used in the proposed inverters. After that, the traditional multilevel inverters are demonstrated, including diode-clamped, capacitor-clamped, and H-bridge multilevel inverters (HCB). Finally, two different Pulse Width Modulation (PWM) schemes are presented for Multilevel Inverter Topologies. For simulation studies and prototype implementation, phase-shifted PWM scheme is used to maintain uniform SOC without the need of carrier wave rotating process, which simplifies the drive circuits and further reduces the cost.

1.5.1 Basic Converter Blocks

The power converter is a solid state device, which converts one form of electric power to another to meet certain specific application needs. Switching voltage converters

operate by applying PWM and hence the current flow through the voltage converter without huge dissipation in power. The PWM control the output voltage with a constant frequency and variable duty cycle. Fig. 7 shows circuit topology of half-bridge DC/DC converter. Once the upper switch *S* conduct, output voltage V_{AB} equals dc link voltage V_d. However, when *S* is turned off, the output voltage equals zero. Therefore, the average value of the output voltage is $V_{AB}=d* V_d$, where *d* is the duty ratio. The duty ratio is defined as the ratio of the conducting time of *S* to one switching period *T*, i.e., $d= t_{on}/T$. Fig. 8 shows the output voltage and its average value when V_d= 400V and *d*= 0.625.

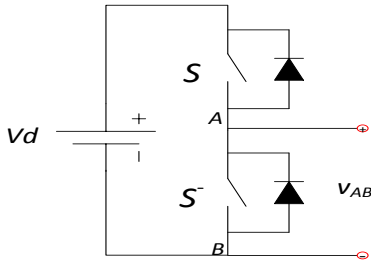


Fig. 7. Half-bridge circuit block.

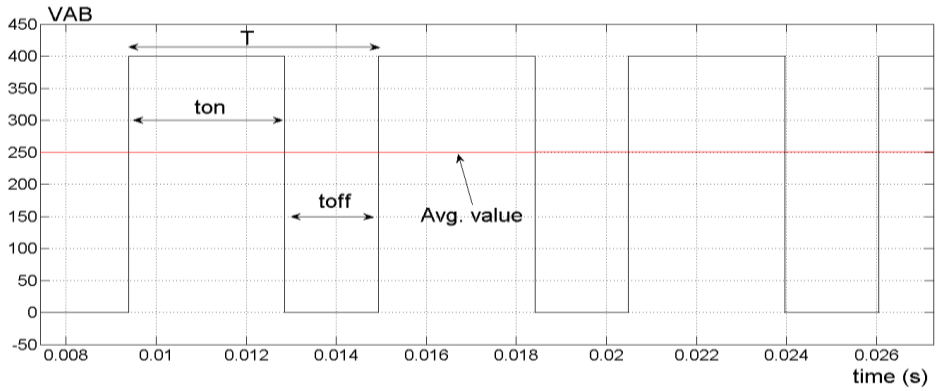


Fig. 8. Output waveform for half-bridge converter: V_d= 400V and *d*= 0.625.

Fig. 9 shows a single-phase H-bridge Converter (HBC). It consists of two converter legs with two semiconductor switches in each inverter leg. IGBTs are normally used for high voltage applications. The input dc link voltage V_d is typically constant, whereas the output ac waveform V_{AB} is adjusted by using PWM techniques. Fig. 10 shows the output voltage

V_{AB} that swings between ± V_d by applying sinusoidal PWM techniques, which will be discussed in detail in Section 1.5.3.1. To complete the positive half-cycle of the output voltage, S_1 and S_4 are turned on. While S_3 and S_2 are used to conduct negative half-cycle at the output terminals.

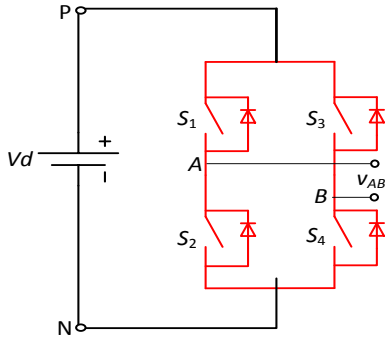


Fig. 9. Single-phase H-bridge inverter.

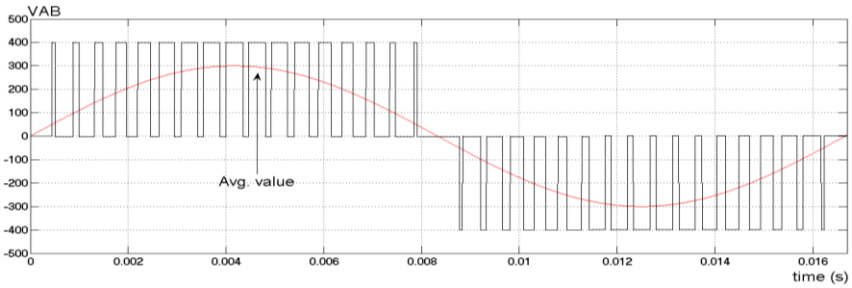


Fig. 10. Output waveform of an H-bridge inverter: V_d=400, fundamental frequency= 60 Hz, carrier frequency=1080 Hz.

The power circuit of a typical three-phase six-switch inverter is shown in Fig. 11. One input dc source is used as the common dc link for the three-phase system. This circuit consists of identical three single-phase half-bridge converters. To achieve three-phase balance operation, the output voltages of those half-bridge converters are out of phase by 120° from each other. When the upper switches S_1, S_2, and S_3 in inverter legs *a*, *b*, and *c* are switched on, the lower switches S_2, S_4, and S_6 operate in a complementary manner and thus are turned off to prevent short-circuiting the dc source. The six-switch converter line-to-line V_{AB} waveform voltage is V_{an} - V_{bn}, which has the same output waveform as that from the H-

bridge inverter in Fig. 10. Other voltage waveforms V_{BC} and V_{CA} can be determined in the same way. However, these basic converters are used as basic building blocks in the proposed multilevel inverters.

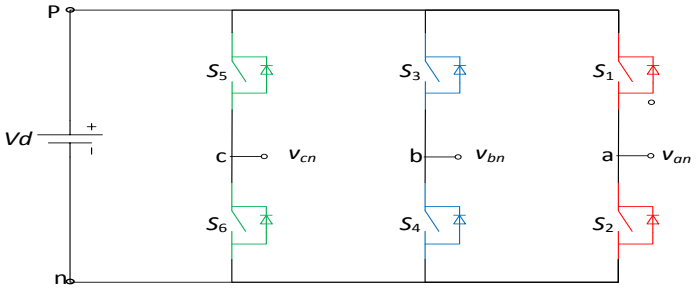


Fig. 11. Three-phase inverter.

1.5.2 Multilevel Inverter Topologies

At medium and/or high voltage levels, in most cases it is hard to connect a single power semiconductor switch directly to the gird [17]. Multilevel inverters have become the workhorse in grid-connected applications. These technologies are employed to provide power with low cost, reduced total harmonic distortion (THD), reduced dv/dt, optimal size, and low electromagnetic interference (EMI). Based on the literature review in Section 1.3, multilevel inverter topologies can be classified into the following groups: common dc link; cascaded separate dc sources; isolated topologies; interconnected three phase, Hybrid HB, Cascaded M-level, and other topologies, as shown in Fig. 12. One of the proposed inverters is an isolated inverter while the second inverter can be classified as an m-level inverter.

The fundamental inverters or converters (or building block units) can be two/three voltage levels only, and hence these basic units need to operate at high frequency to reduce the THD percentage in the output waveforms. As a result, semiconductor-switching devices suffer from high switching losses. To overcome this drawback, the concept of multilevel

topology was proposed. The cascaded H-bridge multilevel inverter was the first multilevel structure proposed by R. H. Baker and L. H. Bannister in 1975 [128]. After that, A. Nabae introduced the neutral-point-clamped in 1981 [129]. A few of years later, Meynard T. A. recommended another fundamental multilevel inverter, which called capacitor-clamped in 1992 [130]. Those traditional multilevel inverters can be classified into two main groups: namely common dc source and cascaded separate dc sources topologies.

1.5.2.1 Common DC Source Multilevel Inverters

In some applications, only one dc power supply (fuel cell or battery pack) is desirable. The common dc source multilevel inverters have been used in motor drives and used in static VAR compensation.

Fig. 13 (a) shows three-phase diode-clamped five-level inverter, which employs clamping diodes and a series connection of capacitor to generate ac voltage waveforms with multiple voltage steps. It is also identified as neutral point clamped (NPC). The diodes in a NPC inverter clamp the voltage and the capacitors at the output are in series to achieve higher multilevel output waveforms. As a result, each switch stands only with one capacitor voltage [48]. Nevertheless, the inverter has a problem of capacitor- unbalance voltage issue and a huge number of clamping diodes when the number of voltage level is high [22]. In addition, the reverse recovery of clamping diodes becomes a major design challenge if the inverter runs under pulse-width modulation (PWM) for high voltage and power applications [17].

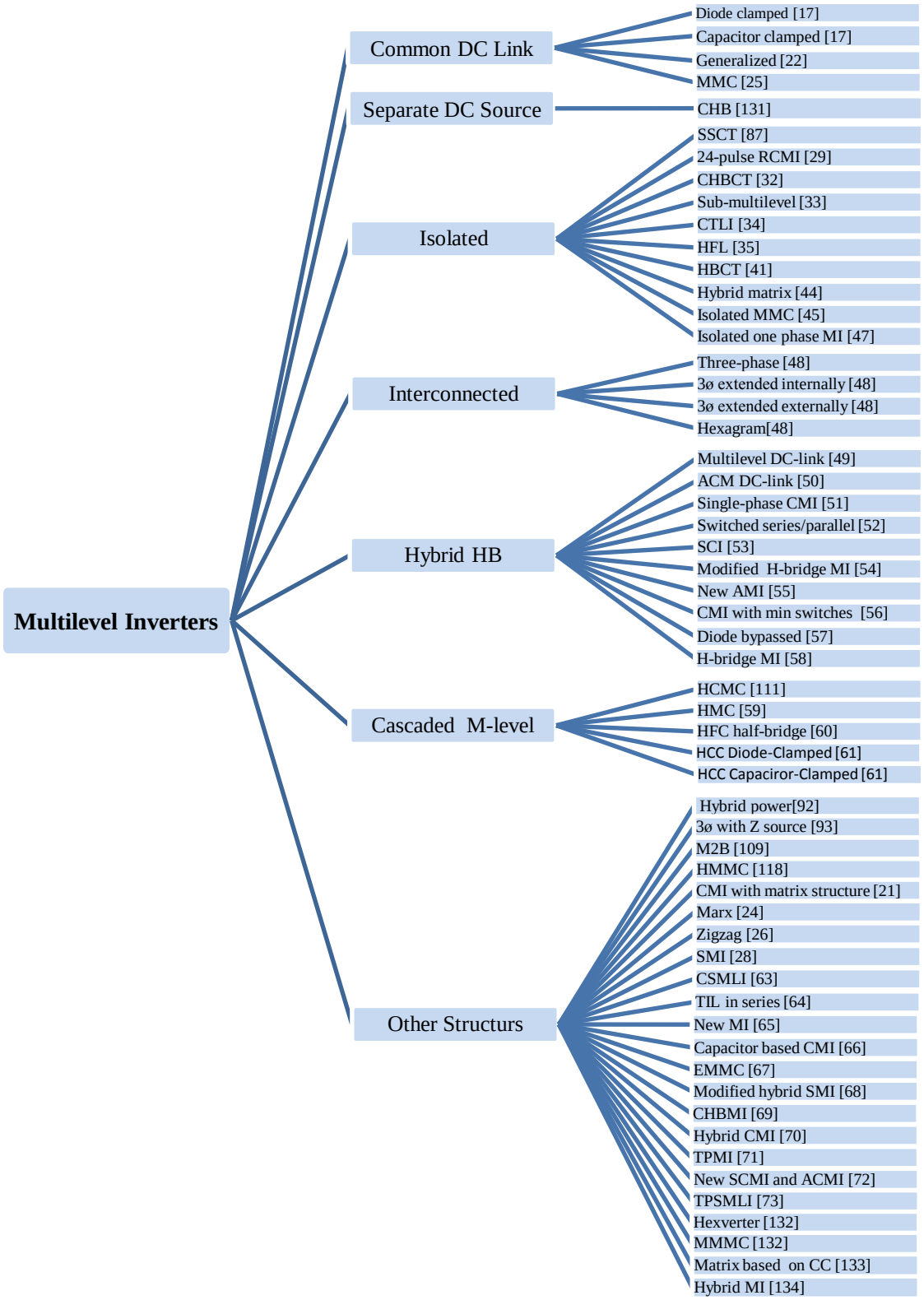


Fig. 12. Classification of multilevel converters.

Fig. 13 (b) shows the single-phase configuration of a five-level flying capacitor inverter, the capacitors are employed to clamp the voltage across switches in a similar clamp mechanism of diode-clamped inverter, but with more capacitors needed. Thus, the size of this type of inverters will get big quickly when the number of voltage-level increases. Moreover, this type of inverter needs complicated control strategies to regulate the floating capacitor voltages [48].

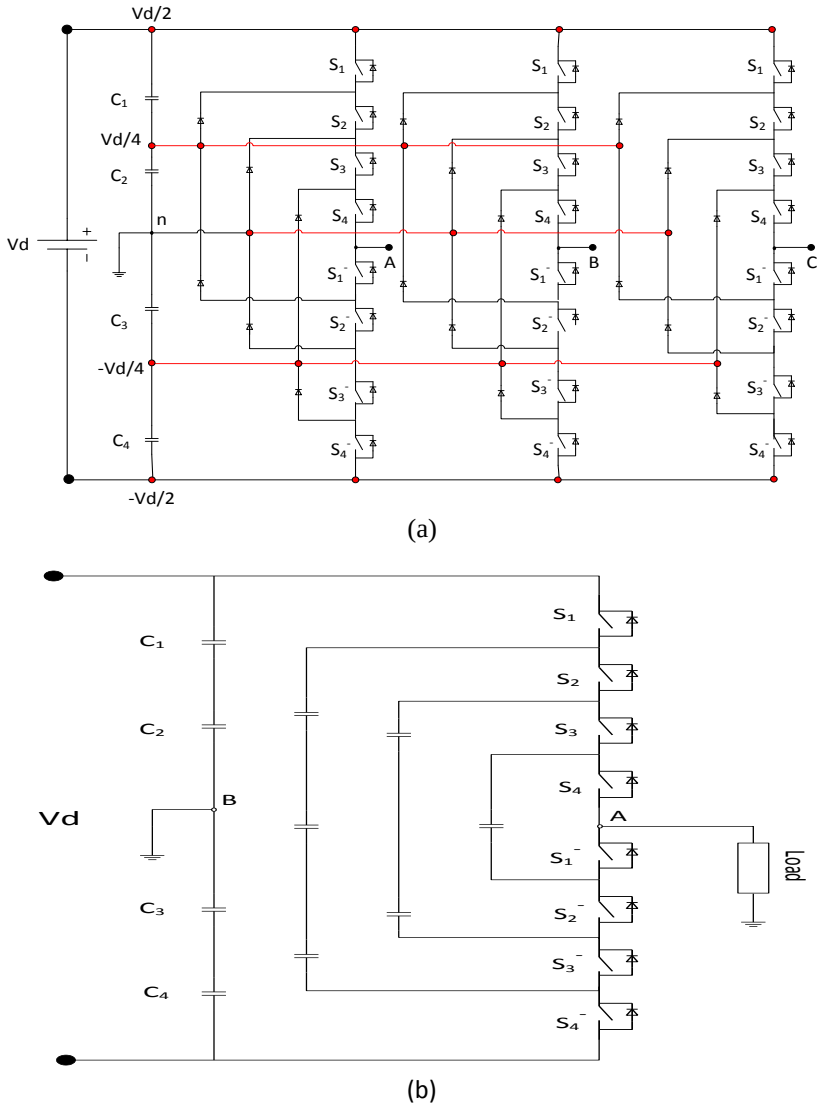


Fig. 13. Common dc source multilevel inverters: (a) Three-phase diode-clamped, and (b) Single-phase capacitor-clamped.

1.5.2.2 Cascaded H-bridge Multilevel Inverter

In the last decades, several multilevel inverter topologies including cascaded inverters are suggested to realize high output voltage and power. Separate dc source multilevel inverters are suitable for battery-energy storage systems. These topologies allow controlling the power of each battery module/cell individually, which increases reliability and battery system utilization. One of the most known multilevel inverters, which needs separate dc sources, is the Cascaded H-bridge (CHB) multilevel converter. A circuit illustration of a three-phase nine-level CHB inverter is shown in Fig. 3.14. The CHB inverter topology has a modular structure and uses fewer components compared with common dc source inverters.

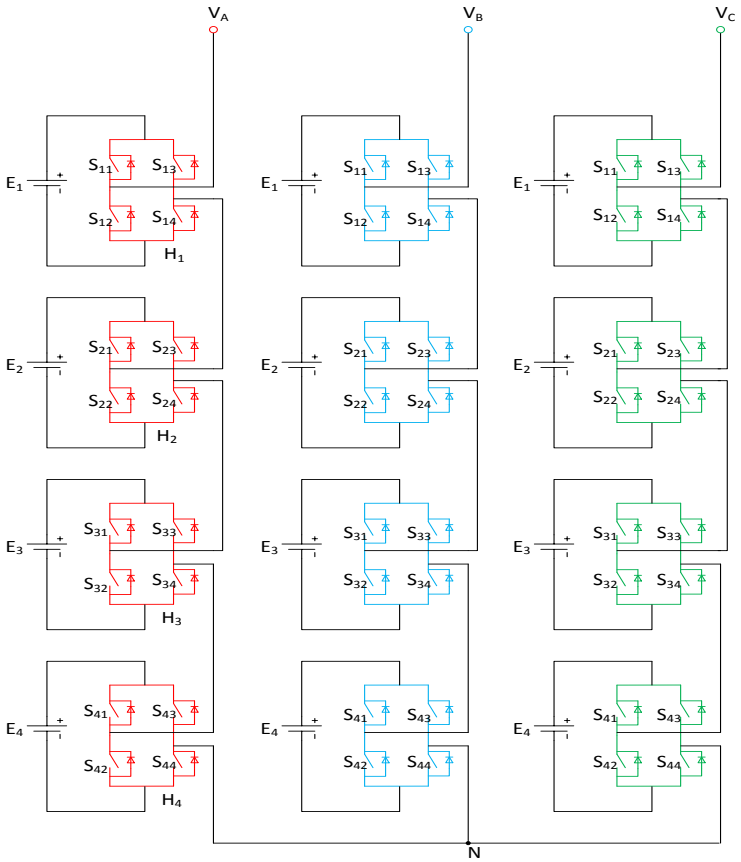


Fig. 14. Nine-level cascaded H-bridge inverter.

Unlike traditional 48 pulse-inverters, the CHB inverter does not need connection transformers [95], which normally are bulky, heavy and expensive. The H-bridge modules are typically linked in cascade on output ac side to elevate voltage and reduce harmonic distortion. In real applications, the output voltage of CHB inverter and the manufacturing cost determine the number of cascaded power modules of H-bridge inverters [74]. In CHB multilevel topology, all dc sources are isolated in a way that each power supply feeds an H-bridge inverter. The dc sources in battery-energy storage systems are battery modules/cells, which allow the battery management system to control each battery module individually to achieve uniform the SOC for the battery strings during charge/discharge processes.

For the inverter in Fig. 14, all three strings have the same output waveforms but with 120° phase shift between any two phases. However, the phase voltage is simply the sum of the voltages of the H-bridge building blocks in each phase, which is the voltage at each inverter terminal (*A*, *B*, or *C*) with respect to the inverter neutral point *N*, i.e., $V_{ph}= V_{H1} + V_{H2} + V_{H3} + V_{H4}$. V_{Hi} (i=1, 2, 3, 4) are controlled by the upper switches in the corresponding H-bridge converters (i.e., S_{11}, S_{13}, S_{21}, S_{23}, S_{31}, S_{33}, S_{41} and S_{43}). To generate the positive half cycle, S_{11}, S_{14}, S_{21}, S_{24}, S_{31}, S_{34}, S_{41}, and S_{44} are connected. Likewise, switches S_{13}, S_{12}, S_{23}, S_{22}, S_{33}, S_{32}, S_{43}, and S_{42} are turned on to carry out negative half-cycle. For simplicity, Table 3 shows some and not all switching states for nine voltage levels which are ±4*E*, ±3*E*, ±2*E*, ±*E*, and 0. However, the highest voltage level ±4*E* can be produced by only one state. From Table 3, some voltage-level steps are produced by more than one switching state, which offers flexibility in the switching design.

Table 3 Voltage steps and some switching states of a nine-level CHB converter.

Output phase voltage	Some upper switches states								H-bridges voltage terminals			
	S_{11}	S_{13}	S_{21}	S_{23}	S_{31}	S_{33}	S_{41}	S_{43}	V_{H1}	V_{H2}	V_{H3}	V_{H4}
4E	1	0	1	0	1	0	1	0	E	E	E	E
-4E	0	1	0	1	0	1	0	1	-E	-E	-E	-E
3E	1	0	1	1	1	0	1	0	E	0	E	E
	1	0	0	0	1	0	1	0	E	0	E	E
	1	1	1	0	1	0	1	0	0	E	E	E
-3E	0	0	0	1	0	1	0	1	0	-E	-E	-E
	0	1	0	0	0	1	0	1	-E	0	-E	-E
	0	1	1	1	0	1	0	1	-E	0	-E	-E
2E	0	0	1	0	0	0	1	0	0	E	0	E
	1	1	1	0	1	1	1	0	0	E	0	E
	1	0	0	1	1	0	1	0	E	-E	E	E
-2E	0	1	0	1	0	0	1	1	-E	-E	0	0
	1	1	0	0	0	1	0	1	0	0	-E	-E
	1	0	0	1	0	1	0	1	E	-E	-E	-E
E	0	0	0	0	0	0	1	0	0	0	0	E
	1	1	1	1	1	1	1	0	0	0	0	E
	1	0	0	1	1	1	1	0	E	-E	0	E
-E	0	0	0	0	0	0	0	1	0	0	0	-E
	1	1	1	1	1	1	0	1	0	0	0	-E
	0	1	1	0	0	0	0	1	-E	E	0	-E
0	1	1	1	1	1	1	1	1	0	0	0	0
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	1	0	1	0	0	1	0	1	E	E	-E	-E

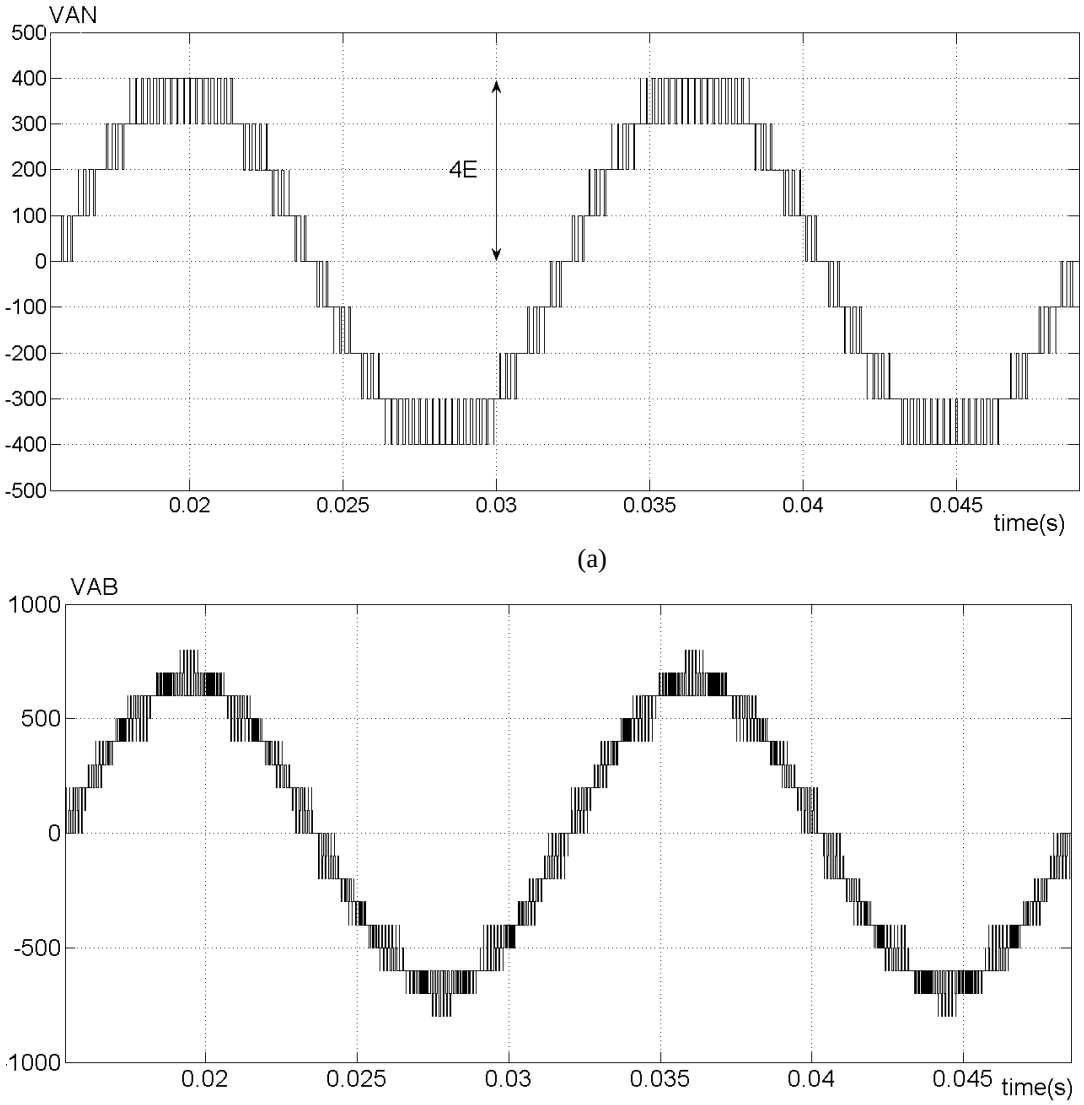


Fig. 15 CHB nine-level inverter: (a) Phase voltage, and (b) Line voltage.

The number (m) of voltage steps in a cascaded H-bridge multilevel converter is found as following

$$m = (2H + 1) \tag{1.2}$$

where H is the number of H-bridge cells per phase. Fig. 15 (a) and (b) show the resultant phase V_{AN} and line $V_{AB} = V_{AN} - V_{BN}$ voltages, respectively. It is clear that line-to-line output waveform has more voltage levels due to the phase shift between phase and line-to-line voltages (i.e., 30°) and hence line-to-line has less harmonic components (less THD%).

1.5.3 Switching and Control Strategies

Power converters convert voltage, current, and frequency with the help of switching techniques, which are used in industrial applications to deliver their required energy. Pulse Width Modulation (PWM) signals are pulse trains with a fixed frequency and adjustable pulse width.

1.5.3.1 Sinusoidal Pulse Width Modulation Technique

PWM modulation techniques are used to control power delivery by changing the average of output power. Fig. 16 illustrates the fundamental concept of the sinusoidal pulse-width-modulation scheme. The fundamental-reference signal waveform for output voltage is derived by amplitude modulation index (m) as following:

$$m = \frac{\hat{v}_m}{\hat{v}_{cr}} \tag{1.3}$$

Where $\hat{v}_m$ and $\hat{v}_{cr}$ are the peak values of the modulating and carrier waves, respectively. The frequency modulation index is defined by

$$m_f = \frac{f_{cr}}{f_m} \tag{1.4}$$

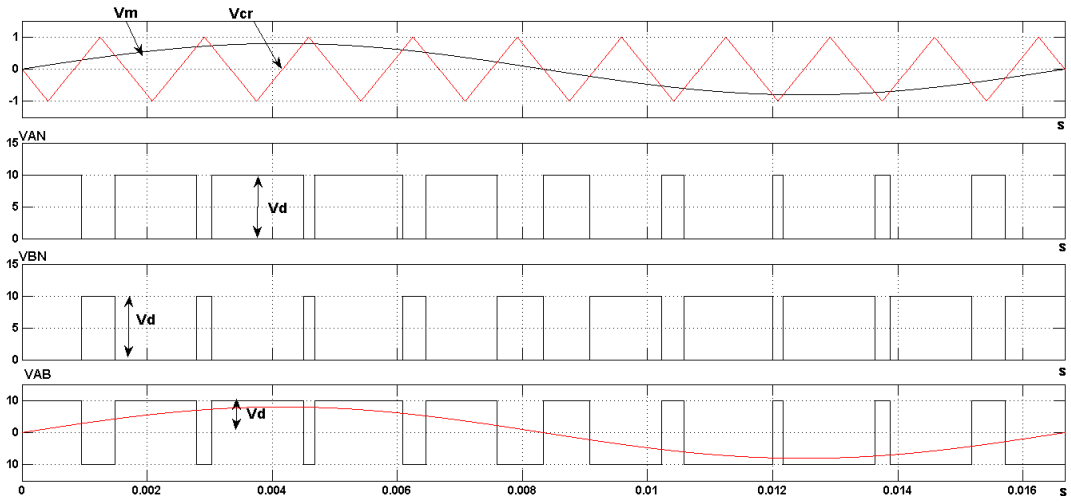


Fig. 16. Sinusoidal pulse width modulation technique.

In Fig. 9, the on-state time of switches is controlled by comparing the triangle waveform with the modulating reference signal. The upper switch S_1 in converter leg-A is connected when $v_m \geq v_{cr}$ and likewise S_1 is turned off when $v_{cr} > v_m$. To avoid short circuit between the dc link terminals, the lower switch S_2 operates in a complementary manner with respect to the upper switch. The resultant inverter terminal voltage V_{AN} is the same as the dc voltage V_d. In case of $v_m < v_{cr}$, S_2 is connected and hence S_1 is off, which leads to $V_{AN} = 0$, as shown in Fig. 16.

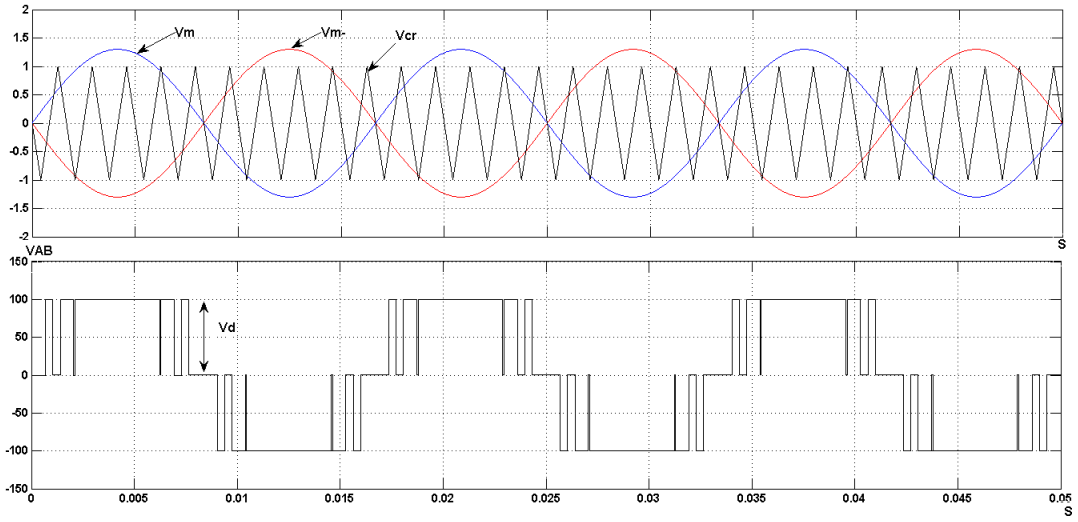


Fig. 17. Over-modulation (m=1.3).

Over-modulation takes place when m is greater than one. Fig. 17 illustrates an example of over-modulation with m= 1.3. For the duration of over-modulation, the number of pulses in the output waveform is reduced and hence, increases low-order harmonics amplitude. The output waveform becomes a square wave if modulated signal v_m is much greater than v_{cr} carrier signal [74]. In real applications, the over-modulation technique is not used specifically for output voltage with low voltage-level because of the difficulty in filtering out the low-order harmonics, caused by the nonlinear relationship between the fundamental component and m.

1.5.3.2 PWM Scheme for Multilevel Inverter Topologies

The multicarrier PWM modulation techniques for multilevel converters are categorized into two groups: phase-shifted and level-shifted schemes. Both modulation techniques can be applied to the proposed multilevel inverters in this work.

1.5.3.2.1 Phase-Shifted PWM Modulation Scheme

A multilevel inverter with *m* voltage levels needs (*m* -1) carrier signals with only one sinusoidal modulating wave or (*m*-1)/2 in case of using two sinusoidal modulating waves. In the phase-shifted PWM scheme, the carrier signals have the same peak-to-peak amplitude and frequency while there is a phase displacement between any two neighboring triangle waves, which can be obtained as follows:

$$\emptyset_{cr} = 360°/(m - 1) \tag{1.5}$$

The modulating wave is a sinusoidal wave with adjustable frequency and amplitude, which is dependent on the actual application requirements. In battery storage systems, the frequency of the modulating signal is fixed while the amplitude is varying to control the SOC for each individual battery module. The gating waves are produced by comparing the carrier waves with the modulating waves. Fig. 18 demonstrates the idea of the phase-shifted PWM scheme for a CHB converter with five-levels (i.e., *m*=5), where two carrier signals are required to have a $\pi/2$ phase shift between them. In Fig. 18, only the phase-A with modulating wave v_m, and v_{m-} are plotted for simplicity. The lower switches are not shown in Fig. 18 because they are working in a complementary manner when compared to the corresponding upper switches.

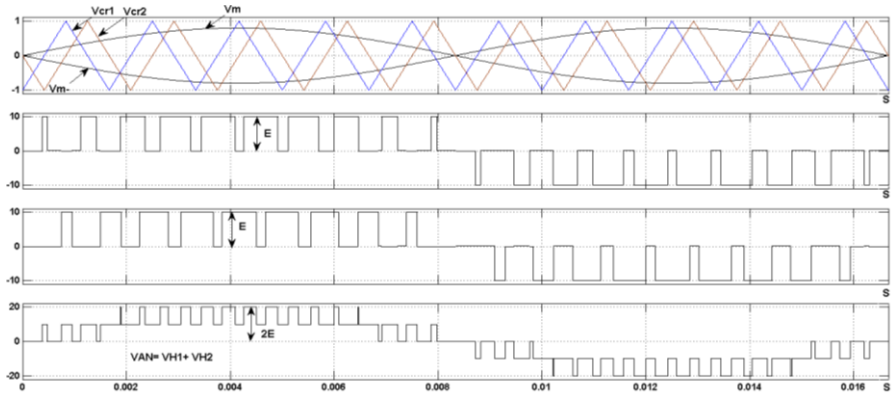


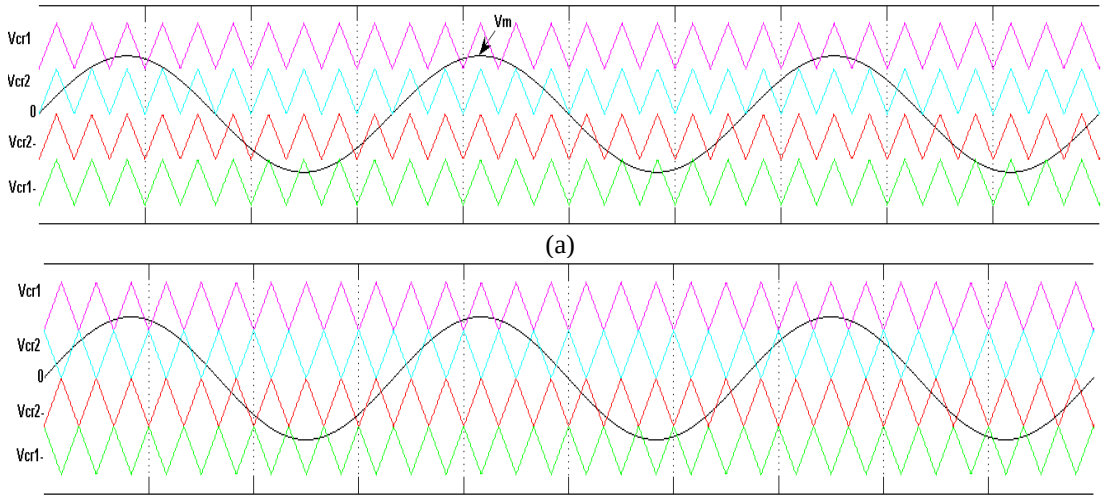
Fig. 18. Five-level CHB inverter with phase-shifted PWM modulation scheme (m=0.8, m_f=10, f_{cr}=600 and f_m=60 Hz).

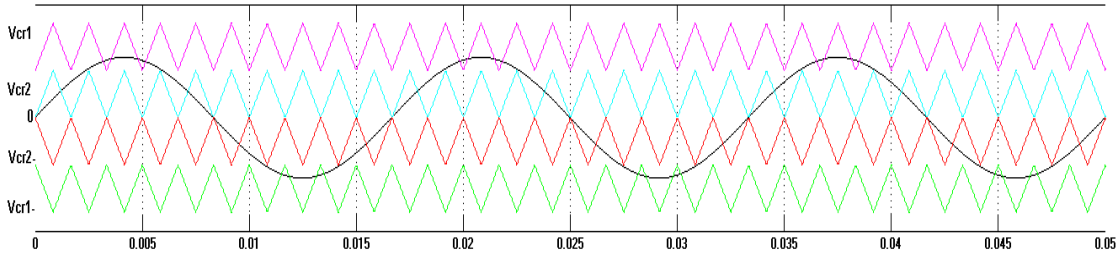
1.5.3.2.2 Level-Shifted PWM Modulation Scheme

Level-shifted PWM modulation technique needs m-1 number of carrier signal waveforms. Like the previous PWM scheme, all the signal waveforms are the same in peak and frequency. The carrier signals are distributed among the vertical-axis as shown in Fig. 19. In the level-shifted PWM method, m_f is fixed as in the phase-shifted PWM technique while the modulation index can be given by

$$m = \frac{\hat{V}_m}{\hat{V}_{cr}(m-1)} \quad \text{for} \quad 0 \leq m \leq 1 \tag{1.6}$$

where $\hat{v}_m$, and $\hat{v}_{cr}$ are the peak value of the reference signal and carrier wave, respectively.





(c)

Fig. 19. Five-level converter: three techniques for level-shifted PWM scheme (a) In-phase disposition (IPD), (b) Alternative phase opposite disposition (APOD), and (c) Phase opposite disposition (POD).

The multicarrier scheme of level-shifted pulse width modulation can be classified into three different techniques that are illustrated in Fig. 19. In the phase disposition (IPD) scheme shown in Fig. 19 (a), the triangle carrier signals have the same phase and amplitude. In Fig. 19 (b), the triangle signals are in reverse disposition for any adjacent carrier signals, which is called alternative-phase opposite disposition (APOD). The last scheme is called phase opposite disposition (POD), shown in Fig. 19 (c). In this technique, the triangle signals below the horizontal axis have the same phase shift but in reverse disposition with carrier signals above the horizontal axis. However, in terms of harmonic, the IPD level-shifted technique offers the lowest THD percentage values compared to the other level-shifted PWM modulation techniques [74].

CHAPTER 2 ISOLATED MULTILEVEL INVERTER FOR LARGE SCALE BATTERY ENERGY STORAGE SYSTEMS

This chapter introduces a new inverter topology for control and management of large-scale battery energy storage systems to achieve uniform SOC operation. The proposed inverter is an isolated multilevel inverter that can be used for high voltage and high power applications such as integrating battery storage systems and alternative energy sources to the power grid. The proposed cascaded multilevel inverter is operated with one or separate dc sources by cascading power transformers. The core building blocks in the multilevel inverter are the six-switch three-phase converters that are controlled using PWM phase-shifted scheme for harmonic reduction. Simulation studies are carried out to verify the performance of the proposed multilevel inverter.

2.1 Proposed Isolated Multilevel Inverter

2.1.1 H-bridge Cascaded Transformer Topology

Cascaded multilevel inverters have become one of the most interesting solutions for medium and high voltage applications but with a need for separate dc sources for each phase. New families of isolated cascaded multilevel inverters have been proposed such as asymmetric cascaded multilevel inverter [35], combined H-bridge cascaded transformer (CHBCT) multilevel inverter [32], cascaded multilevel inverter (CMI) [74], hybrid CMI inverter [74], and sub-multilevel inverter [33]. Fig. 20 shows the topology of a three-phase H-bridge cascaded transformers (HBCT) multilevel inverter with a single dc power voltage source. This scheme is used to add output voltage levels up by increasing the number of transformers instead of increasing the number of dc voltage sources. Moreover, the HBCT inverter provides a filtering effect of harmonic components due to the leakage reactance of

the cascaded transformers [33] and also provides the electric isolation between the output and source [32].

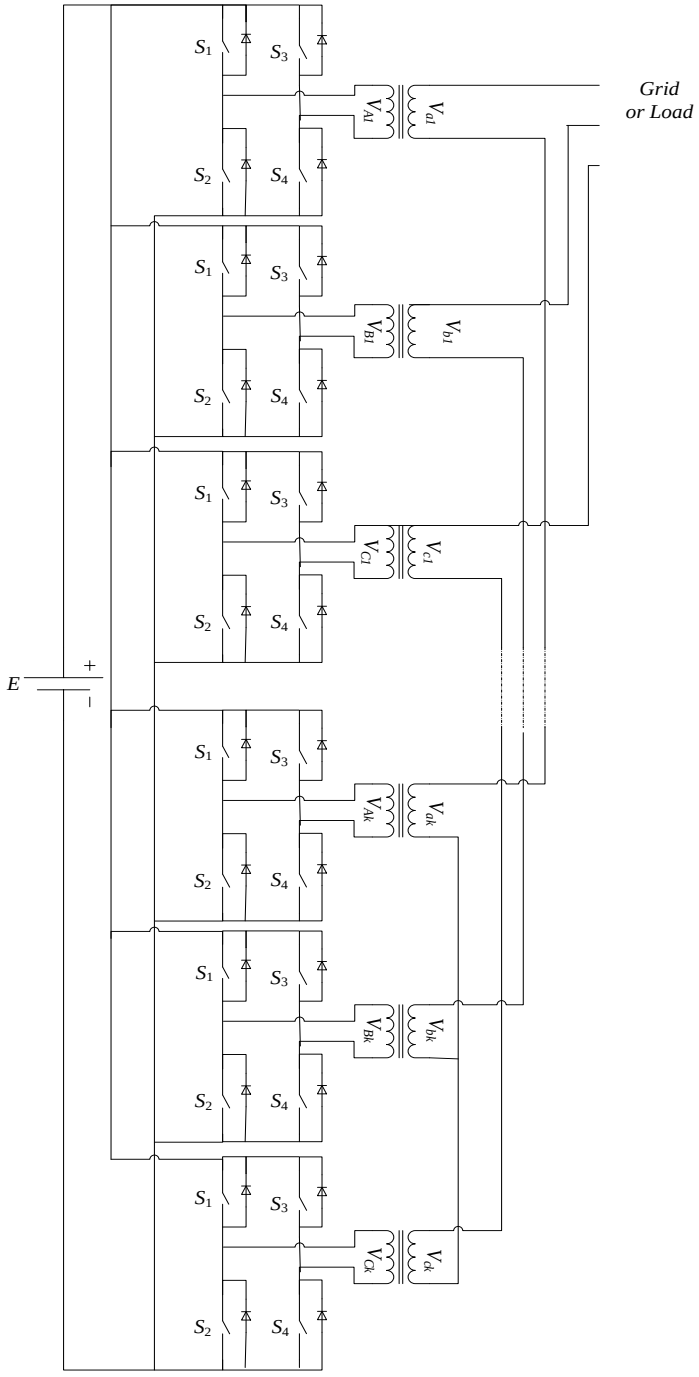


Fig. 20. Topology of a three-phase H-bridge cascaded transformer (HBCT) multilevel inverter [135].

In the HBCT inverter, the primary terminals of the windings of the transformers are connected to the H-bridge inverters to synthesize output voltage of $+V_{dc}$, 0 V and $-V_{dc}$ while the terminals of the secondary windings are connected in series to elevate the output voltage. The amplitude of the output voltage is determined by the turn ratios of the cascaded transformers and the input dc voltage. Hence, this inverter can operate in either symmetric or asymmetric mode to synthesize the steps of the output voltage [33]. The maximum number of phase voltage levels in a symmetric HBCT inverter is given by:

$$m = 2K + 1 \tag{2.1}$$

where *m*, *K* are the number of voltage levels and the number of cascaded transformers, respectively. The output voltage can be obtained by summing the voltages across the secondary terminals of the cascaded transformers.

$$V_o = \sum_{i=1}^{K} V_i \tag{2.2}$$

2.1.2 Six-Switch Cascaded Transformer (SSCT) multilevel inverter

A new cascaded transformer based multilevel inverter topology with separate dc sources is proposed here. The building blocks in the proposed multilevel inverter are six-switch three-phase inverters, not the single-phase H-bridge converters used in the HBCT shown in Fig. 20. Fig. 21 shows the circuit topology of the six-switch cascaded transformer (SSCT) multilevel inverter. One of the advantages of using three-phase converters as building blocks is that a *dq* frame based control can be used, which is simpler and can provide better performance compared with controls based on alternating single-phase signals. Moreover, this also eliminates the issues of single-phase pulsating power, which can cause

detrimental impacts on certain dc sources such as fuel cells and batteries. The leakage reactance of the cascaded transformers can also help filter harmonics.

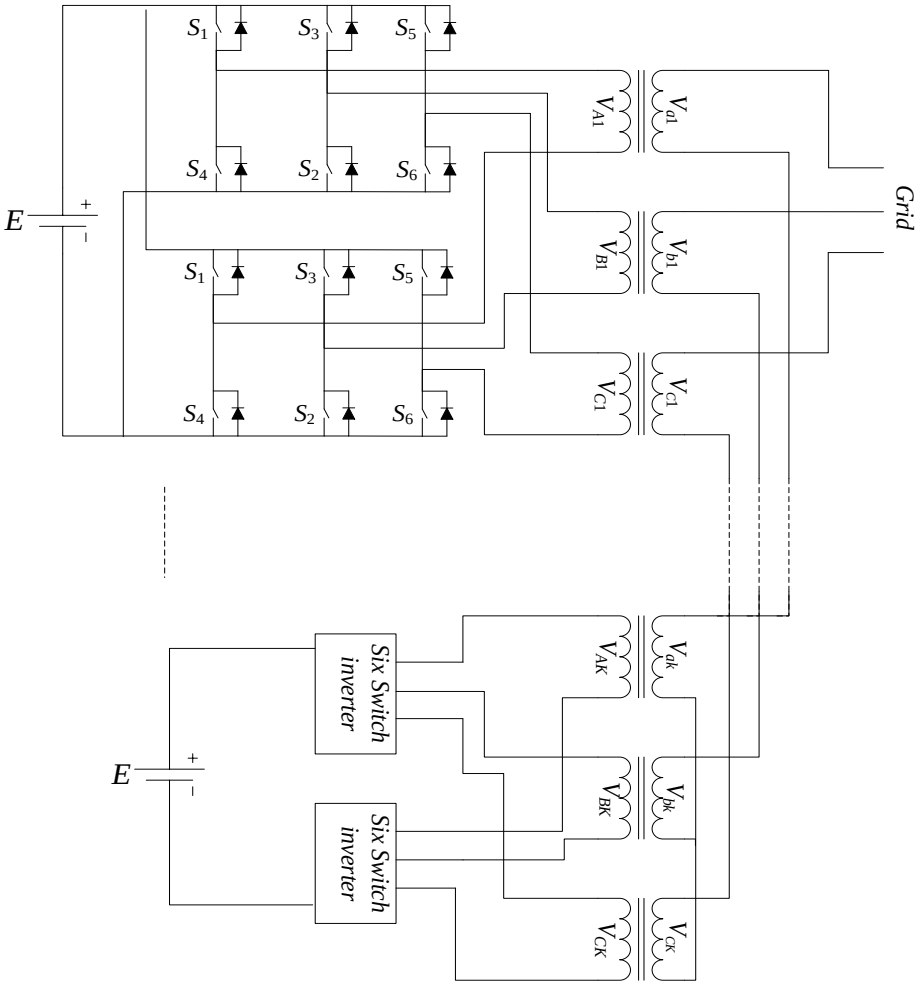


Fig. 21. Circuit topology of the SSCT inverter.

Fig. 22 shows the circuit diagram of a basic cell of the proposed inverter. Each cell consists of two fundamental building blocks (i.e., six-switch inverters) which are connected to the primary terminals of a power frequency transformer (turn ratio =1) to generate three voltages at the output side: $+E$, 0 V and $-E$. The two inverters are controlled by a 12-pulse PWM technique (unipolar PWM drive technique of three-phase inverter) where the upper inverter is driven by the first 6 pulses while the remaining pulses are used to control the

second inverter. The pulses are generated by comparing a triangular carrier waveform with two sinusoidal modulating waves for each phase which are of the same magnitude and frequency but 180° out of phase. For example, pulses 1, 2, 7 and 8 are used to drive the corresponding switches which are connected to phase-A where S_2 and S_8 are complementary switches for S_1 and S_7, respectively. As a result, S_1 and S_8 work together to perform $+E$ and 0 while S_2 and S_7 are used to provide $-E$ and 0 at output terminals. In other words, the two inverters work together as a complementary device for each other, making it easy to connect them to three single phase transformers.

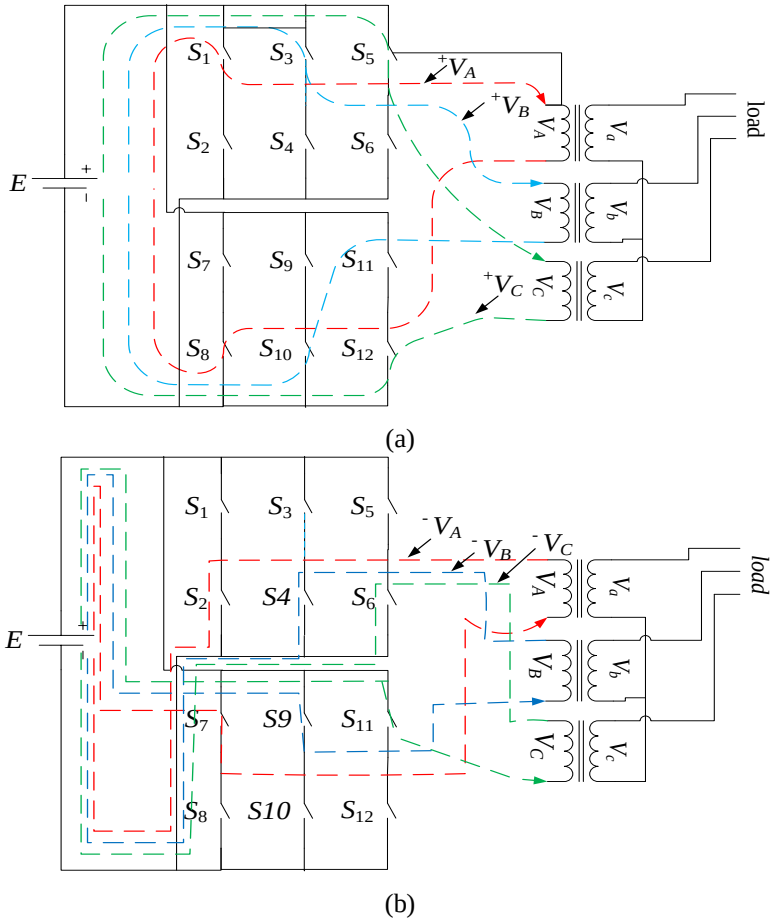


Fig. 22. Basic cell of the SSCT inverter in the circuit topology: (a) Three phase positive level, and (b) Three phase negative level.

Well established carrier based PWM modulation techniques (such as phase-shifted or level-shifted modulation) for multilevel inverter can be used for the SSCT inverter. In this dissertation, the phase-shifted scheme is used to control the SSCT inverter to reduce harmonics in the output voltage. All the basic cell building blocks are connected to separate dc sources and all the secondary terminals of the basic units are connected in series to elevate the output voltage. As a result, the voltage level is increased by cascading more transformers. The peak of the output voltage is determined by the turn ratios of the cascaded transformers, the number of voltage levels and the input dc voltages. The SSCT inverter can operate in either symmetric or asymmetric mode. If all the turn ratios are the same, the inverter is known as a symmetric multilevel inverter and the resulting output ac voltage could swing from $+K\alpha E$ to $-K\alpha E$ where K, α are the number of the cascaded transformers and the turn ratio, respectively. The output phase voltage can be determined by summing the voltages across the secondary terminals of the cascaded transformers, which can be described by (2.2) as well. The number of voltage levels in the symmetric SSCT inverter is also given by (2.1).

It is noticed that the structure of SSCT inverter in Fig. 21 acts similarly to the three-phase HBCT multilevel inverter while the proposed inverter has the ability to reduce the number of semiconductor switches and cascaded transformers. The transformer at the last stage can be removed if electric insolation is not needed and the transformer turn ratio is not large. As presented in Fig 23, for the last stage in the cascaded string, one transformer per-phase and one six-switch inverter block can be removed. Furthermore, in the other stages, certain six-switch inverter blocks can be removed as well. So, one six-switch block can be removed for each stage except one stage that still needs to have two inverter blocks to

provide a complementary path (e.g., block A' B' C' in Fig. 23) for all the remaining six-switch inverter blocks. Compare to the topology in Fig. 23 (a), Fig. 23 (b) shows a nine-level of compact SSCT inverter with only 5 six-switch inverters. The compact structure has only one complementary six-switch inverter black. Thus, only one dc source or one dc link can be used. The compact inverter can be realized for second-hand battery packs/modules connected in series. For example, old EV batteries (15 kWh/40kW) can still have a sizable amount of capacity left (up to 75%) that are not applicable for electric vehicle applications [136]. In the near future, the number of these retired batteries will increase. Hence, a huge waste if not utilized in their secondary applications, such as BESSs for grid applications.

The modulating signals are three-phase sinusoidal waves with fundamental system frequency (60 Hz), and the gate signals are generated by comparing the modulating waves with the carrier waves. The inverter block(s) at each stage is driven by the PWM phase shifted scheme and every carrier wave requires a phase displacement (φ) as follows:

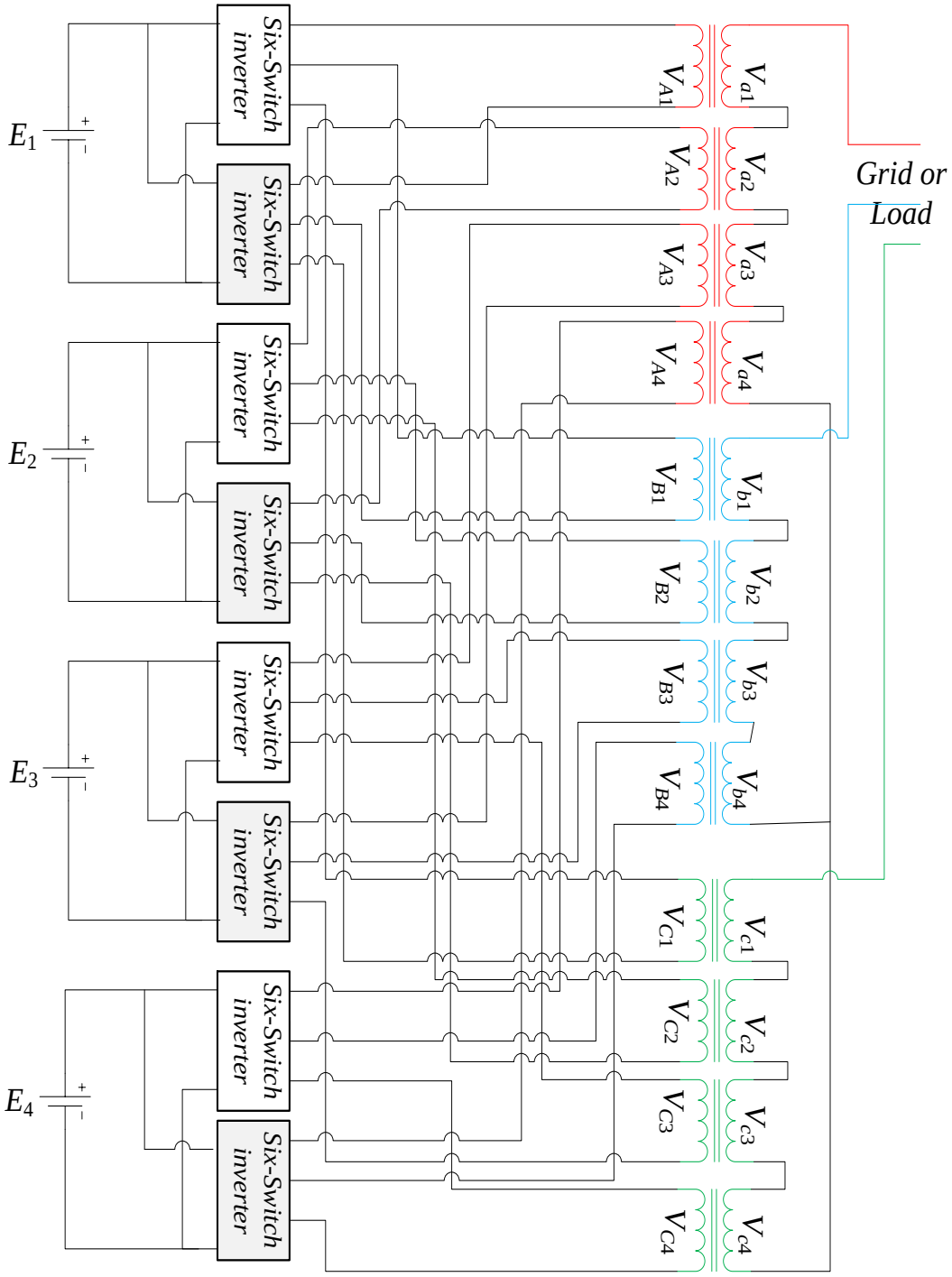
$$\varphi = \frac{360^{\circ}}{(m-1)} \tag{2.3}$$

where *m* is the voltage level. If there is only one inverter block in a stage, 6-pulse modulation scheme is used; otherwise, 12-pulse modulation scheme is applied. To minimize the harmonic in the compact SSCT inverter, the complementary six-switch inverter can be driven by a phase shift of the following:

$$\varphi = \frac{1}{4}\frac{(m-5)*360^{\circ}}{(m-1)} \tag{2.4}$$

For example, *m* equals 9 for the proposed topology (Fig. 23-b) and to reduce the THD%; the complementary six-switches inverter is controlled at $\varphi = 45^{\circ}$. However, the number of

inverter components is primarily determined by the harmonic requirements, size and the manufacturing cost.



(a)

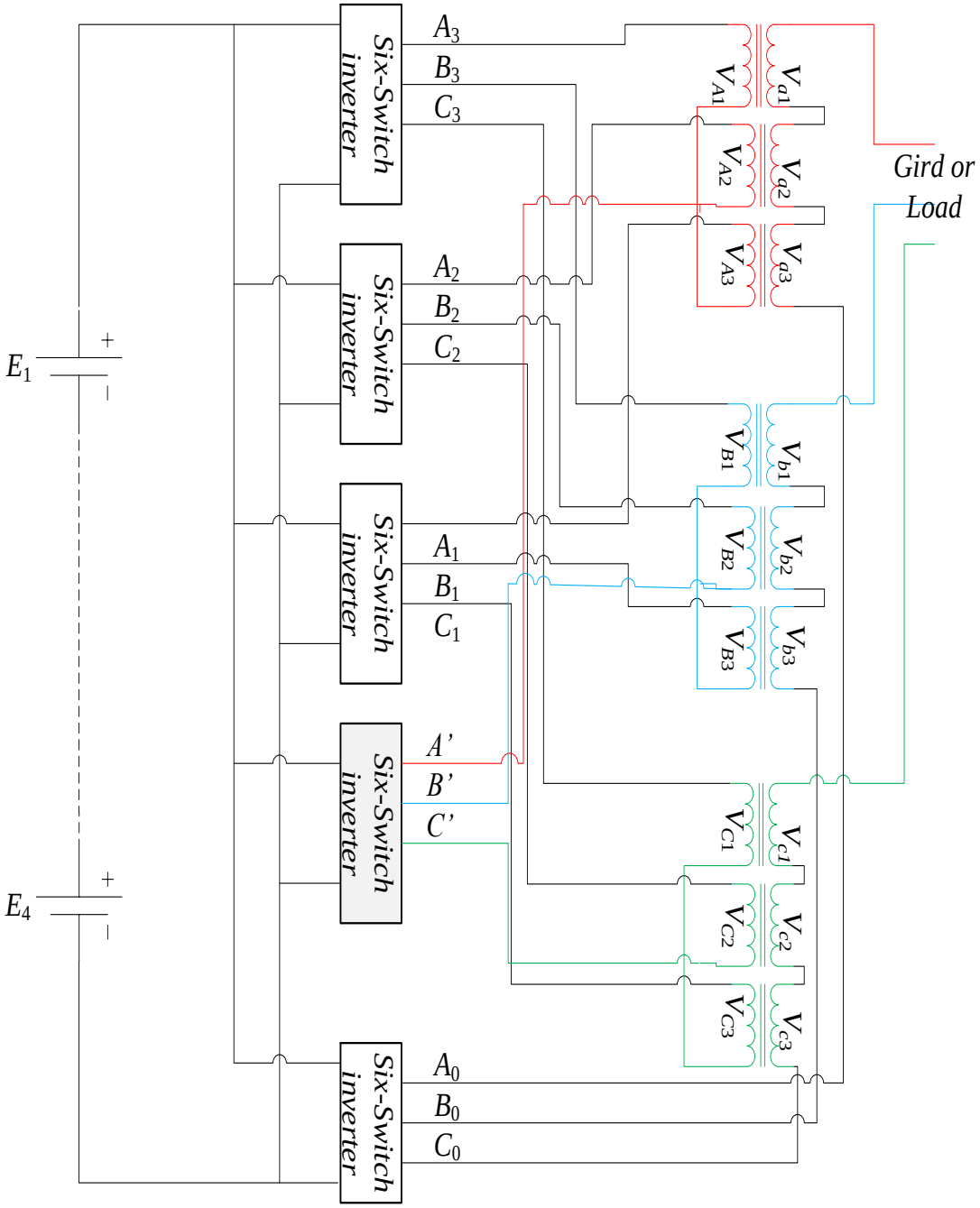


Fig. 23. Nine-level SSCT inverter: (a) SSCT inverter, (b) The compact SSCT inverter.

2.2 SOC Weighted Real and Reactive Power Control

The real and reactive powers delivered to or provided by the grid are determined by the amplitude and angle of the output voltage of the cascaded inverter if the grid voltage is

assumed constant. For a given reference value of real and reactive power P and Q, the magnitude (V) and phase angle (β) of the inverter output can be obtained as:

$$V = \left[\frac{Z^2}{E^2}(P^2 + Q^2) + E^2 + 2PZ\cos(\theta_z) + 2QZ\sin(\theta_z) \right]^{\frac{1}{2}} \tag{2.5}$$

$$\beta = \theta_z - \cos^{-1}\left(\frac{ZP}{EV} + \frac{E}{V}\cos(\theta_z) \right) \tag{2.6}$$

where $Z = \sqrt{R^2 + X^2}$, $\theta_z = \tan^{-1}(X/R)$. $R + jX$ is the coupling impedance and the grid voltage is assumed to be $E\angle 0°$. β will be negative when the grid charges battery. The corresponding *dq* component values of the voltage can be obtained through *abc/dq* transformation as follows:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = T_{abc/dq0} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = T_{abc/dq0} P^{-1} \left(\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \right) = T_{abc/dq0} P^{-1} \left(\begin{bmatrix} V\angle\beta \\ V\angle(\beta - 120°) \\ V\angle(\beta + 120°) \end{bmatrix} \right) \tag{2.7}$$

where P^{-1} is the inverse phasor transform, that obtains the time expression of a variable from its phasor representation.

As shown in Fig. 24 and discussed before, each battery or basic cell has two six-switch three-phase interfacing converters. The overall system's real and reactive power control is achieved via the control of each basic cell. When the quantities (V_d, and V_q) in the *dq* frame for the overall system are determined by the reference values of P and Q, the corresponding *dq* frame values are distributed among all the battery module interfacing converters based on their SOCs to achieve the overall real and reactive power control. For discharging control (delivering power back to the grid)

$$V_{d,k} = V_d \frac{SOC_k}{\sum_{k=1}^{N} SOC_k}$$
$$V_{q,k} = V_q \frac{SOC_k}{\sum_{k=1}^{N} SOC_k} \tag{2.8}$$

$V_{d,k}$ and $V_{q,k}$ are the corresponding dq values for the basic cell inverter of battery k. For charging control,

$$V_{d,k} = V_d \frac{1 - SOC_k}{\sum_{k=1}^{N} (1 - SOC_k)}$$
$$V_{q,k} = V_q \frac{1 - SOC_k}{\sum_{k=1}^{N} (1 - SOC_k)} \tag{2.9}$$

V_0 will be zero for balanced three phase systems, on which our discussion is mainly focused.

The proposed control strategy can not only achieve the real and reactive power flow control, but also regulate the SOC of batteries in the system. The batteries with higher SOCs will be controlled to share more power delivery in the discharging mode while the batteries with lower SOCs will be controlled to be charged with more power in the charging mode. Hence, a uniform SOC distribution among the batteries in the system can be eventually achieved. It is also worthwhile to mention that the system can provide reactive power support under either charging or discharging mode.

The overall control system block diagram for the inverter is also given in Fig. 24. The "*dq* Reference Signal Computation" block calculates the magnitude and angle of the filtered output voltages of the inverter and then converts them into *dq* voltage reference signals, $V_{d,q,(k)}$. The "*abc/dq* Transformation" block takes the (*abc* coordinate) current and

voltage values from the voltage and current meters and converts them into dq values. The outer voltage controller takes the error signals between the actual output voltage in the *dq* frame ($v_{d,q,(k)}$) and the reference voltage ($V_{d,q,(k)}$), and generates the current reference signals ($I_{d,q,(k)}$) for the current control loop. The inner current controller produces the *dq* control signals, which are distributed among all the battery module interfacing converters based on their SOCs to achieve the overall real and reactive power control. The control signals are converted back into the *abc* coordinates through the "*dq/abc* Transformation" block. These signals are used to control a pulse width modulator to produce the proper pulses for all the 12×*N* inverter switches, which will shape the inverter output voltage to achieve the desired real and reactive power flow. It should be noted that the above control method relies on the accurate estimation of the state of charge [13, 137, 138].

2.3 Simulation Studies

Fig. 24 shows the block diagram of a battery energy storage system with the proposed nine-level cascaded inverter. In the proposed scheme, each dc source (battery) can be managed individually in principle. The unique differences between the suggested inverter and the traditional CHB ones are: (1) the three six-switch inverters connected to the same battery will be controlled together as a core block in the system; (2) the modulation strategy for battery converters are similar to others, making the control and gate drive circuits relatively simpler; (3) the three-phase strings can be controlled together as a single three-phase inverter by using the *dq* transformation technique; and (4) highly reliable operation. The batteries are integrated together via their interfacing converters, not connected directly.

If there is anything wrong with a battery module, the overall system can still be operated at a down-graded mode by isolating the faulty battery via its six-switch inverters.

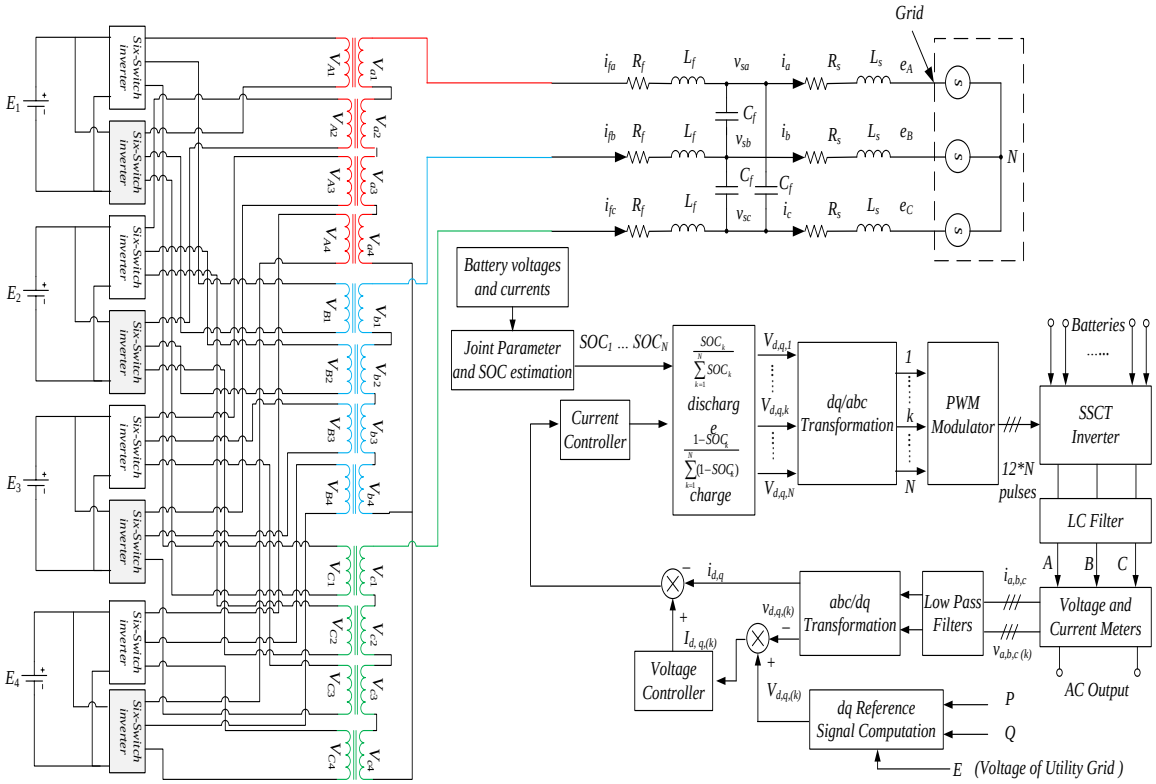
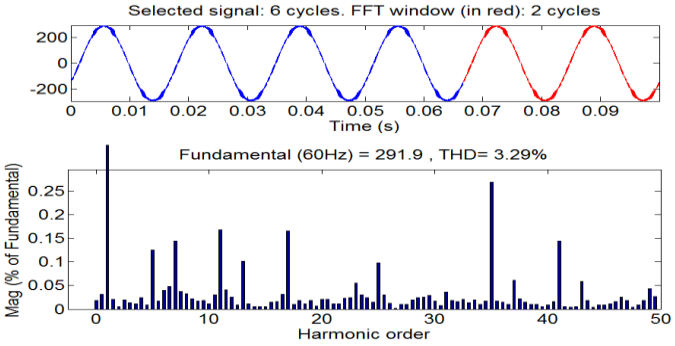
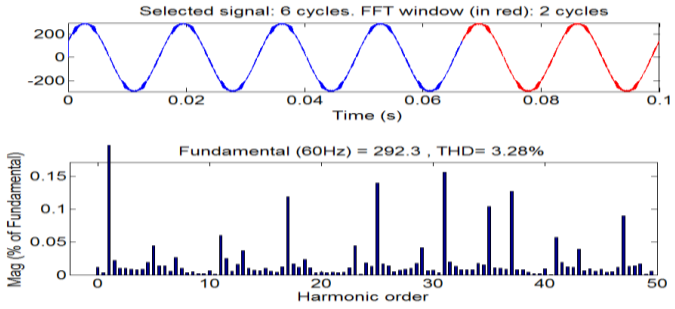


Fig. 24. SSCT converter for integrating battery energy storage system with SOC weighted power control.

Fig. 25 shows the output voltage waveforms and the corresponding THD% for both the proposed and the HBCT multilevel inverters. The carrier frequency is set to 1080 Hz. The result shows that SSCT has the same performance in THD% compared to the traditional topology. For the compact structure, it is interesting to note that the proposed compact inverter has smaller low order (below 16th) harmonic components although the total THD% is higher. It is relatively easier to filter high-frequency harmonics than low order ones. As shown in Fig. 26(b), the output THD% of the proposed inverter is close to the HBCT with a 0.5 kVar capacitive load added.

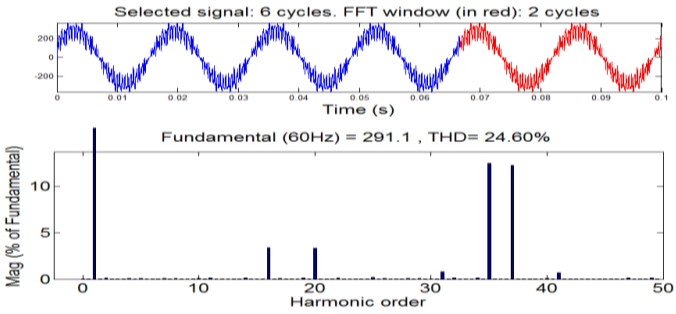


(a)

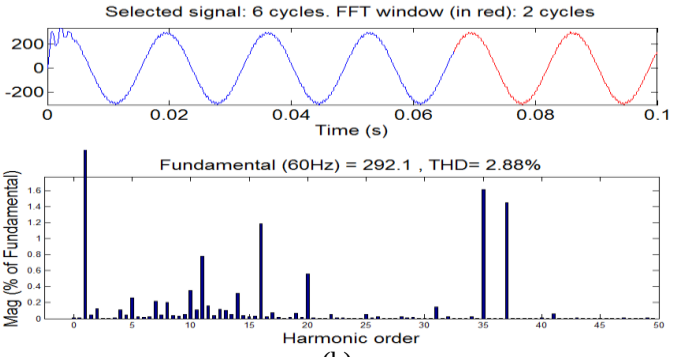


(b)

Fig. 25 Output voltage waveforms: (a) HBCT; and (b) SSCT.



(a)



(b)

Fig. 26. Output voltage waveforms of the compact SSCT inverter: (a) Output voltage without filtering; and (b) Output voltage with 0.5 kVar capacitor.

To verify the performance of the proposed SOC balancing scheme, a BESS of 4

battery packs (0.8kW/2.2Ah) is simulated as shown in Fig. 24. Based on (2.8) and (2.9) methodologies, the control scheme can not only realize the real and reactive power flow control but also the uniform the SOC of batteries in the system. The battery modules with higher SOCs are controlled to share more power delivery in the discharging process while the modules with lower SOCs will be managed to be charged with more power in the charging mode. Hence, a uniform SOC distribution among the batteries in the system can be eventually achieved. Fig. 27 shows the process of balancing SOC during discharge mode where initial SOC conditions of battery modules vary from 100% to 99.25%. Under uniform SOC, the battery modules are loaded equally because the system has only one battery string.

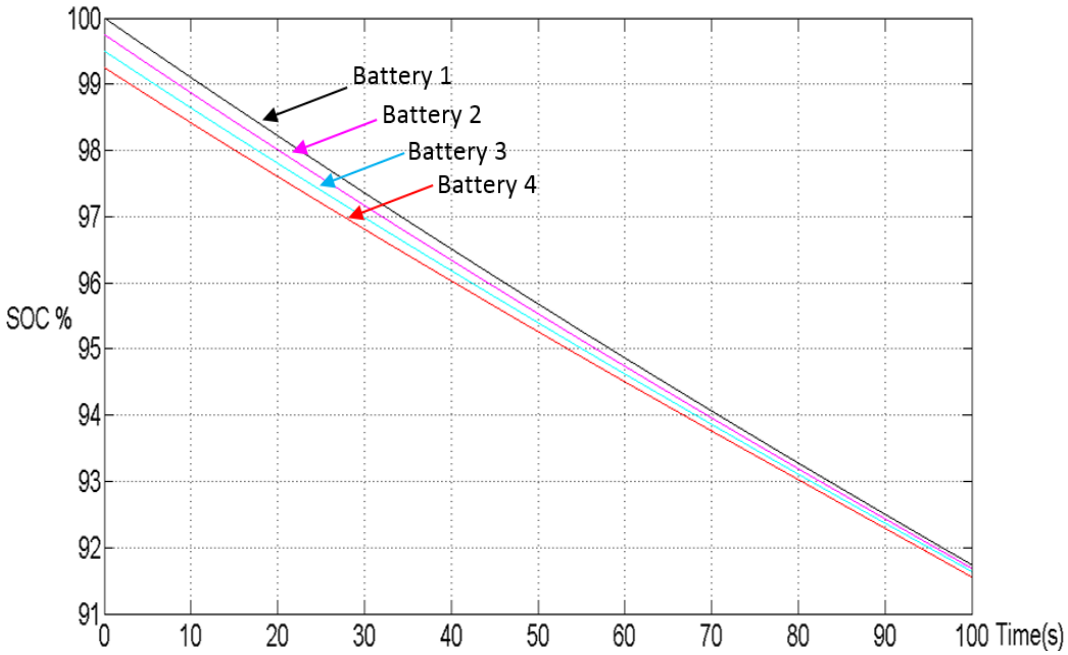


Fig. 27. SOC balancing of modules in the battery string during the discharging process.

CHAPTER 3 NON-ISOLATED MULTILEVEL INVERTER FOR LARGE-SCALE BATTERY ENERGY STORAGE SYSTEMS

This chapter presents a new topology of a cascaded multilevel converter, called Hierarchal Cascaded Multilevel Converter (HCMC). The topology is a hybrid combination of both H-bridge and half-bridge converters which can be cascaded at two hierarchical levels, i.e., the H-bridge level and half-bridge level. A phase-shifted PWM modulation technique is developed for the proposed HCMC with different conduction time for the upper switching devices in the half-bridge circuits to achieve an equal utilization of battery modules/cells. There is no need of carrier wave rotating process, which simplifies the drive circuits and further reduces the cost. The converter has the features of high voltage and high power application capability and modular design for cost reduction and reliability improvement. A uniform SOC profile can be achieved via the proposed converter without adding additional balancing circuits. Furthermore, failed individual battery modules/cells can be bypassed via the converter without bringing down the whole battery system. Simulation and experimental studies have been carried out to verify the performance of the proposed hierarchal cascaded multilevel converter.

3.1 Operation Principle of the Proposed HCMC

For large-scale battery systems, cell/module balancing is important to protect the weaker batteries while to fully utilize the full capacity of the whole battery system. This section introduces a hierarchal converter where a uniform SOC operation is achieved and maintained continuously by controlling individual battery modules/cells.

3.1.1 Circuit Topology

To control individual battery modules/cells, a HCMC consisting of half-bridge converter blocks and H-bridge blocks is proposed. Fig. 7 (in Chapter 1) shows a half-bridge block that is interfaced to an individual module/cell and manages that module/cell. Therefore, individual modules and cells can be managed separately through half-bridge blocks. The half-bridge circuits are cascaded in series and then connected to an H-bridge circuit to form a hybrid multilevel converter. An example configuration of a nine-level HCMC is shown in Fig. 28, where only one H-bridge in a single phase is shown. The H-bridge in the circuit is used to just alternate the dc link output voltage of the cascaded half-bridge blocks. It is worth pointing out that the hybrid circuit in Fig. 28 looks similar to that presented in [16]. However, a different PWM (i.e., a phase-shifted PWM) modulation technique is used in this work, discussed later in this section. Moreover, another cascaded connection can be made at the H-bridge level to meet further needs on high voltage and high power, as shown in Fig. 31.

In Fig. 28, when the upper switches S_1, S_2, S_3, and S_4 in the cascaded half-bridge blocks conduct, the output voltage of the half-bridge blocks h_1, h_2, h_3, and h_4 is V_{h1}, V_{h2}, V_{h3}, and V_{h4} respectively. Hence, the resultant dc voltage is V_{dc}= V_{h1}+V_{h2}+V_{h3}+V_{h4}= $\sum_{i=1}^{4} E_i$. The output phase voltage of the HCMC converter V_{AN} is an alternating voltage that could swing from ($\sum_{i=1}^{4} E_i$) to ($\sum_{i=1}^{4} -E_i$) by using the H-bridge which operates at the fundamental frequency of the reference signal. The other four voltage levels of the dc link are $\sum_{i=1}^{3} E_i$, $\sum_{i=1}^{2} E_i$, E_i, and 0, which correspond to the various switching states summarized in Table 4. It can be observed from Table 4 that some voltage levels can be obtained by more

than one switching state. For example, the voltage level $\sum_{i=1}^{2} E_i$ can be produced by six sets of different switching states, which provide great flexibility for switching pattern. The number of voltage levels in a HCMC multilevel inverter can be found from

$$m = 2h + 1 \tag{3.1}$$

where h is the number of half-bridge cells per phase. The voltage level m is always an odd number for the HCMC multilevel inverter. It is in the same pattern as that of traditional cascaded H-bridge (CHB) multilevel inverters while in other multilevel topologies such as diode-clamped inverters the voltage level can be either an even or odd number.

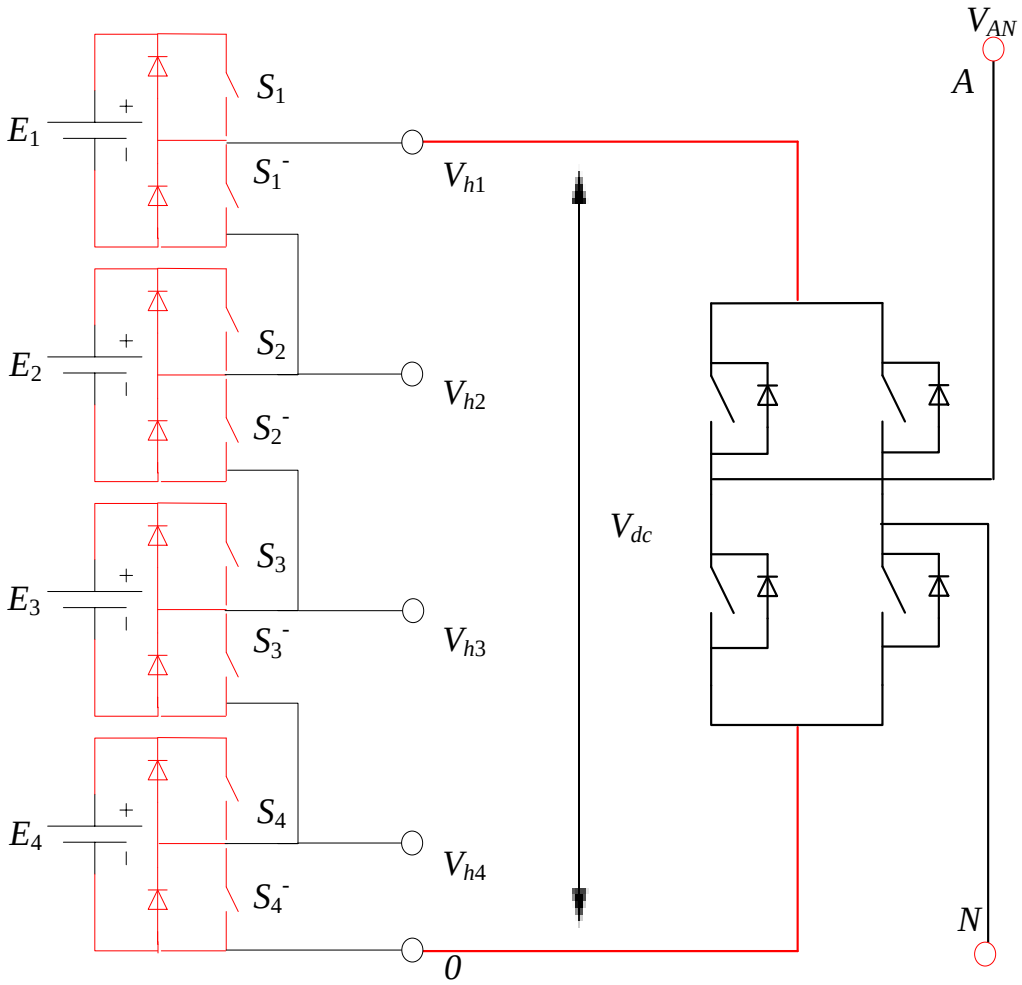


Fig. 28. Topology of a single-phase nine-level HCMC inverter.

3.1.2 Phase-shifted PWM Modulation

In general, a traditional multilevel inverter with m voltage levels requires (m-1) triangular carriers [74], but the cascaded half-bridge cells in the HCMC inverter requires only (m-1)/2 triangular waves. A phase-shifted PWM modulation scheme is developed for the proposed HCMC. By using the phase-shifted multicarrier modulation, the triangular carriers have the same frequency and the same amplitude, but with a phase shift (φ) between any two adjacent carrier waves, which is given in equation (1.5).

Table 4 Voltage steps and switching state of the nine-level HCMC inverter in Fig. 28.

DC Link Voltage	Switching State				half-bridges voltage terminals			
	S_1	S_2	S_3	S_4	V_{h1}	V_{h2}	V_{h3}	V_{h4}
$\sum_{i=1}^{4} E_i$	1	1	1	1	E_1	E_2	E_3	E_4
$\sum_{i=1}^{3} E_i$	0	1	1	1	0	E_2	E_3	E_4
	1	0	1	1	E_1	0	E_3	E_4
	1	1	0	1	E_1	E_2	0	E_4
	1	1	1	0	E_1	E_2	E_3	0
$\sum_{i=1}^{2} E_i$	0	0	1	1	0	0	E_3	E_4
	1	0	0	1	E_1	0	0	E_4
	1	1	0	0	E_1	E_2	0	0
	1	0	1	0	E_1	0	E_3	0
	0	1	0	1	0	E_2	0	E_4
	0	1	1	0	0	E_2	E_3	0
E_i	1	0	0	0	E_1	0	0	0
	0	1	0	0	0	E_2	0	0
	0	0	1	0	0	0	E_3	0
	0	0	0	1	0	0	0	E_4
0	0	0	0	0	0	0	0	0

For the cascaded half-bridge converter blocks, the modulation signals $V_{m,i,x}$ (battery module i in phase *x*, *x*=*a*, *b*, *c*) are the absolute values of the reference voltages that depend

to SOCs of individual battery modules/cells. The gate signals are generated by comparing the absolute values of the reference voltage waves with the carrier signals. If all battery modules have the same output voltage and capacity, Fig. 29 shows the principle of the phase-shifted scheme for the nine-level basic cell converter, where there is a 45° phase displacement between any two neighboring triangular carrier waves. The carrier waves V_{cr1}, V_{cr2}, V_{cr3}, and V_{cr4} are used to generate the gate signals for the upper switches of the cascaded cells h_1, h_2 , h_3, and h_4 in Fig. 28, respectively. The gate signals for all the lower switches in the cascaded half-bridge are not shown since these switches operate in a complementary way with respect to their corresponding upper switches.

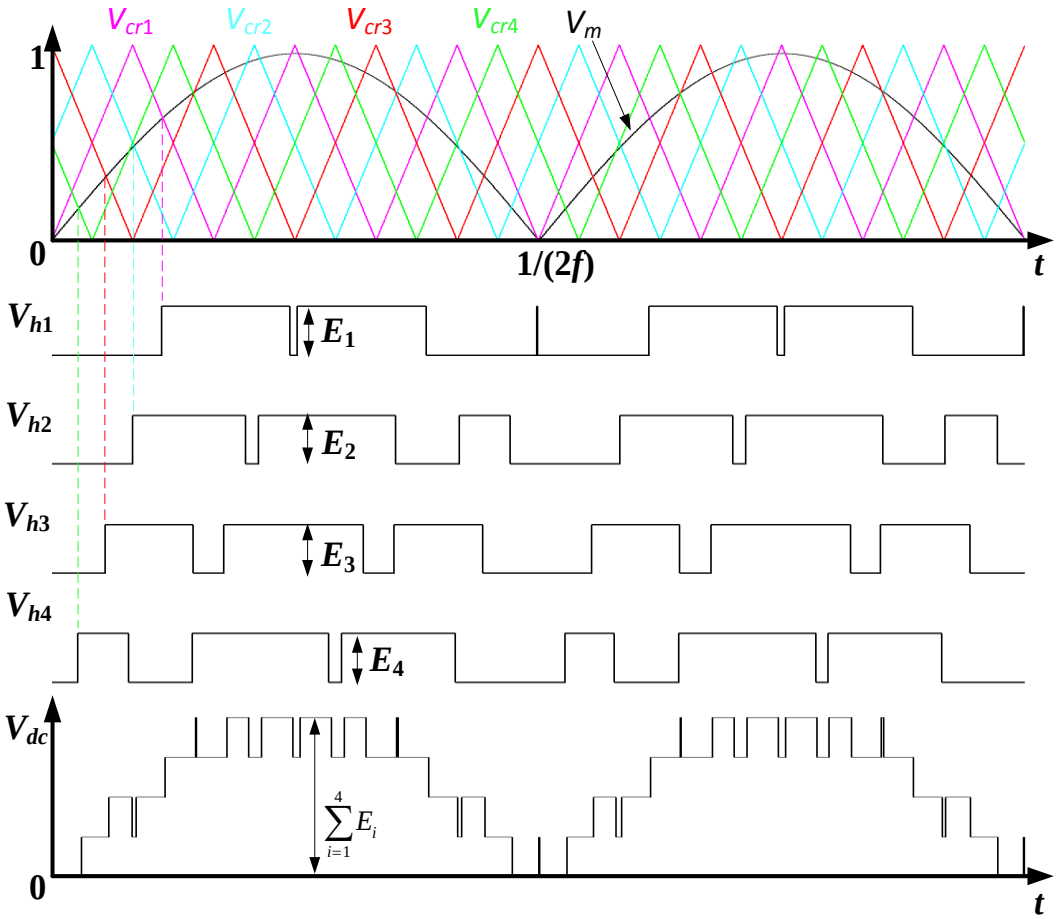


Fig. 29. Phase-shifted PWM modulation for a nine-level HCMC.

As shown in Fig. 29, the gate signals for the upper switches S_1, S_2, S_3, and S_4 in the cascaded blocks h_1, h_2, h_3, and h_4 are generated by comparing V_{cr1}, V_{cr2}, V_{cr3}, and V_{cr4} with Vm. Hence, the resultant voltages V_{h1}, V_{h2}, V_{h3}, and V_{h4} are switched between zero and E_i during the half cycle of the fundamental frequency.

Modulation index can be calculated as

$$m_i = V_{mp}/V_{crp} \tag{3.2}$$

where V_{mp} and V_{crp} are the peak amplitudes of V_m and V_{cr}, respectively. The dc link voltage can be readily obtained as

$$V_{dc} = V_{h1} + V_{h2} + V_{h3} + V_{h4} \tag{3.3}$$

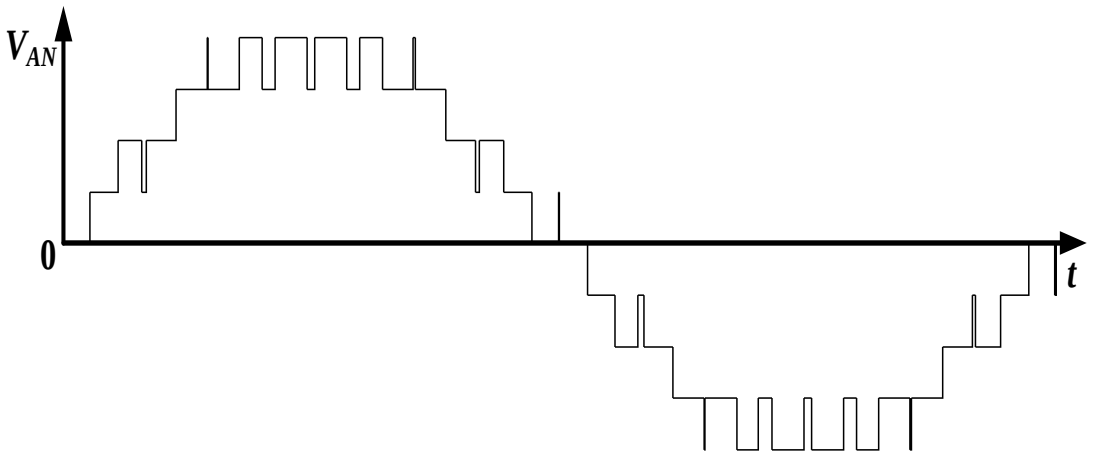


Fig. 30. Output voltage of nine-level HCMC multilevel inverter (m_i=0.95, fundamental frequency= 60Hz, and carrier frequency= 180 Hz).

The H-bridge circuit is used to alternate the dc link voltage Vdc as shown in Fig. 30. The output voltage signal VAN is the nine-level HCMC phase voltage under the condition of a 60 Hz fundamental frequency, a 180 Hz carrier frequency, and a modulation index mi at 0.955. It can be clearly seen that the converter phase voltage waveform is formed by nine

voltage steps: $\pm\sum_{i=1}^{4} E_i$, $\pm\sum_{i=1}^{3} E_i$, $\pm\sum_{i=1}^{2} E_i$, $\pm E_i$, and 0. The magnitude of voltage step is only E_i during the switching between voltage levels, which leads to a low voltage stress.

3.1.3 Hierarchal Cascaded Topology

An example three-phase thirty three-level HCMC is shown in Fig. 31. There are four cascaded half-bridge converters in each H-bridge converter block and there are 4 H-bridge converters cascaded for each single phase. The output of the cascaded half-bridge converters is connected to the dc side of the H-bridge converter. In this topology, each battery module/cell can be involved in producing the output voltage or being bypassed, which can be achieved by simply controlling the switches in the half-bridge converter for each battery module/cell. The charge and discharge power to each battery module/cell can be controlled by controlling the modulation index, which is discussed in detail in Section 3.2. The H-bridge function is to alternate the output of the dc link to produce ac waveforms at the output terminals. The switches in the H-bridge converters need to handle higher voltage and power levels, but are switched at a much lower frequency (i.e., the fundamental frequency). On the other hand, the switches in each half-bridge converter work under lower voltage and power and can be switched much faster. Therefore, MOSFETs can be selected as the switches for the half-bridge blocks while IGBTs can be chosen for the H-bridge converter blocks in the HCMC. Compared to traditional H-bridge multilevel converters, the number of switching devices is reduced specially for large battery systems, which helps simplify the control drive circuits, reduce the total cost, and achieve a smaller size converter.

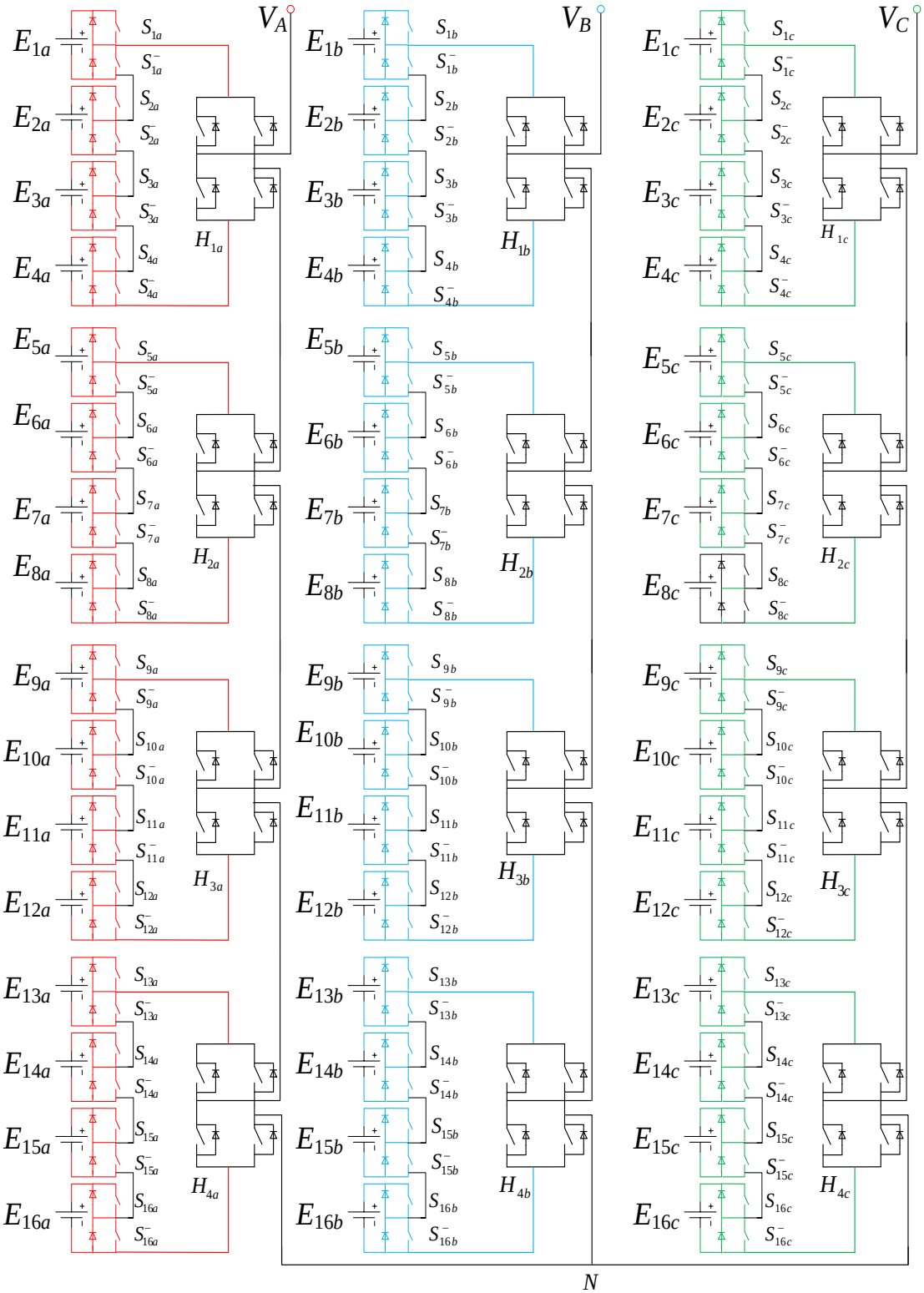


Fig. 31. Topology of a three-phase HCMC with two hierarchical cascaded levels: the half-bridge level and H-bridge level.

3.2 Charging and Discharging Control

The charge and discharge power control of an individual battery module/cell is achieved through the control of the half-bridge converter connected to the module/cell. The charge/discharge power can be regulated by controlling the modulation index $m_{i,x}$ (battery module i in phase x, x=a, b, c) of the switching device of each half-bridge converter. The instantaneous charge/discharge power of the battery module/cell is given by

$$P_{cell,i}(t) = S_{upper,i,x}(t) \times E_{i,x} \times I_{dc} \tag{3.4}$$

where $S_{upper,i,x}$ is the i_x^{th} battery module/cell upper switch states in phase x, x=a, b, c: 1 is ON or 0 is OFF; $E_{i,x}$ and I_{dc} are the voltage of the individual battery module/cell and the battery current of the whole string, respectively. The average power of a battery module/cell is:

$$\bar{P}_{cell,i,x} = m_{i,x} \times E_{i,x} \times I_{dc} \tag{3.5}$$

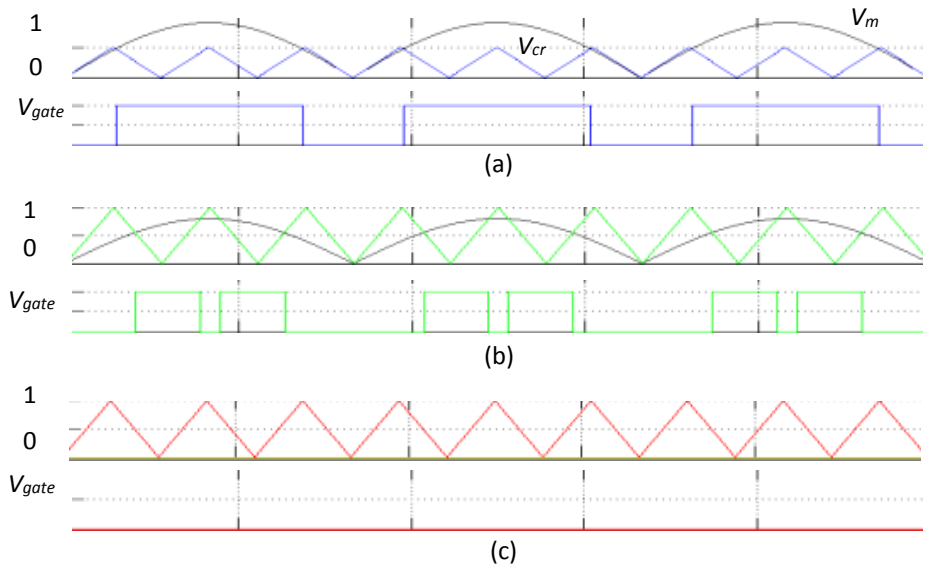


Fig. 32. PWM modulation and gate signals of a upper switch in a half-bridge converter block: (a) Over-modulation ($m_{i,x} > 1$), (b) Example of ($0 < m_{i,x} < 1$) and (c) ($m_{i,x} = 0$).

Hence, the charge or discharge power of each battery module/cell is controlled by regulating $m_{i,x}$ of the corresponding half-bridge converter. Fig. 32 shows different cases of $m_{i,x}$ where it is used to regulate battery power and/or bypass the battery module/cell. For example, in a discharging process, a battery module/cell with a higher SOC can be discharged more even with an over-modulated index $m_{i,x}$ > 1, shown in Fig. 32 (a). Other battery modules/cells with a lower SOC can be controlled to be discharged less with a lower modulation index, 0< $m_{i,x}$ <1. In the charging process, a similar strategy can be carried out. When one or more modules/cells need to be bypassed, the upper switching devices of the half-bridge converters of these battery modules/cells can be turned OFF by simply applying $m_{i,x}$= 0, as shown in Fig. 32 (c) without affecting other modules/cells. However, in this case, the overall phase output voltage with bypassed modules/cells will be reduced. The half-bridge converters of the other healthy battery modules/cells can be controlled to generate a higher voltage to compensate this voltage drop until the damaged battery modules/cells are replaced. Nevertheless, during that period of time, the whole system will be operated at a de-rated power and energy level. The corresponding *dq* component values of the voltage can be obtained through *abc/dq* transformation as shown in (2.7).

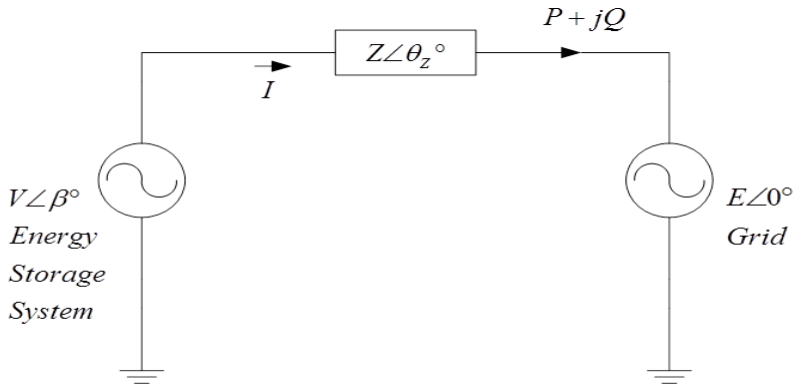


Fig. 33. Single diagram of BESS connected to utility grid.

Fig. 33 shows power flow between energy storage system and utility power grid. The

overall (charge or discharge) power can be regulated by controlling the overall output AC voltage, i.e. the magnitude V and phase angle β. For balance system, the dq component values of HCMC output voltage are given by the following equations:

$$V_d = E_d + \frac{LdI_d}{dt} + RI_d - wLI_q$$
$$V_q = E_q + \frac{LdI_q}{dt} + RI_q + wLI_d \tag{3.6}$$

where E_d, E_q, I_d, and I_q are the dq component values of both power grid voltage E, and inverter current I respectively. Inductance L and resistance R are the components of the coupling impedance. However, the modulating waveform equations of the three-phase system shown in Fig. 34 are given by

$$v_a^* = V\,|sin(\omega t + \beta)|$$
$$v_b^* = V\,|sin(\omega t - 120 + \beta)| \tag{3.7}$$
$$v_c^* = V\,|sin(\omega t + 120 + \beta)|$$

For a given reference value of real and reactive power P and Q, the reference magnitude (V) and phase angle (β) of the inverter output can be obtained from (2.5) and (2.6), respectively. From (2.5) and (2.6), the calculated dq values are given by:

$$Vd_{cal} = \frac{V_{cal}}{E}\cos(\beta_{cal})$$
$$Vq_{cal} = \frac{V_{cal}}{E}\sin(\beta_{cal}) \tag{3.8}$$

The overall battery energy storage system with power controller block diagram for the proposed inverter is shown in Fig. 34. The "dq reference signal computation" block, computes V and β of cascaded converter and then obtains dq reference values. However, $\Delta V_{d,q}$ are added to compensate the error due to grid component measurements i,e., L and R.

The new reference equations can be found by:

$$V_{dref} = Vd_{cal} + \Delta V_q$$
$$V_{qref} = Vq_{cal} + \Delta V_d \tag{3.9}$$

where $\Delta V_q = Q_{ref} - Q_{Grid}, \Delta V_d = P_{ref} - P_{Grid}$. Based on (3.6) and (3.9), the modulating waveforms v_a^*, v_b^*, and v_c^* in Fig. 34 can be found by applying inverse transformation of the following *dq* components:

$$V_d{}^* = E_d + \frac{LdI_d{}^*}{dt} + RI_d{}^* - wLI_q{}^* + \Delta V_q$$
$$V_q{}^* = E_q + \frac{LdI_q{}^*}{dt} + RI_q{}^* + wLI_d{}^* + \Delta V_d \tag{3.10}$$

The overall power demands can be decomposed into the commands at the individual battery module/cell level as

$$P^*_{cell,i,x} = \frac{P_{tot}}{N} + \Delta P_{cell,i,x} \tag{3.11}$$

where P_{tot} is the overall power demand; $P^*_{cell,i,x}$ is the reference value for the i_x^{th} battery module/cell; N is the total number of modules/cells in the system; and $\Delta P_{cell,i,x}$ is the power adjustment for the uniform SOC management and $\sum_{i=1}^{n_x} \Delta P_{cell,i,x} = 0$, and n_x is the total number of battery modules in series for phase *x*.

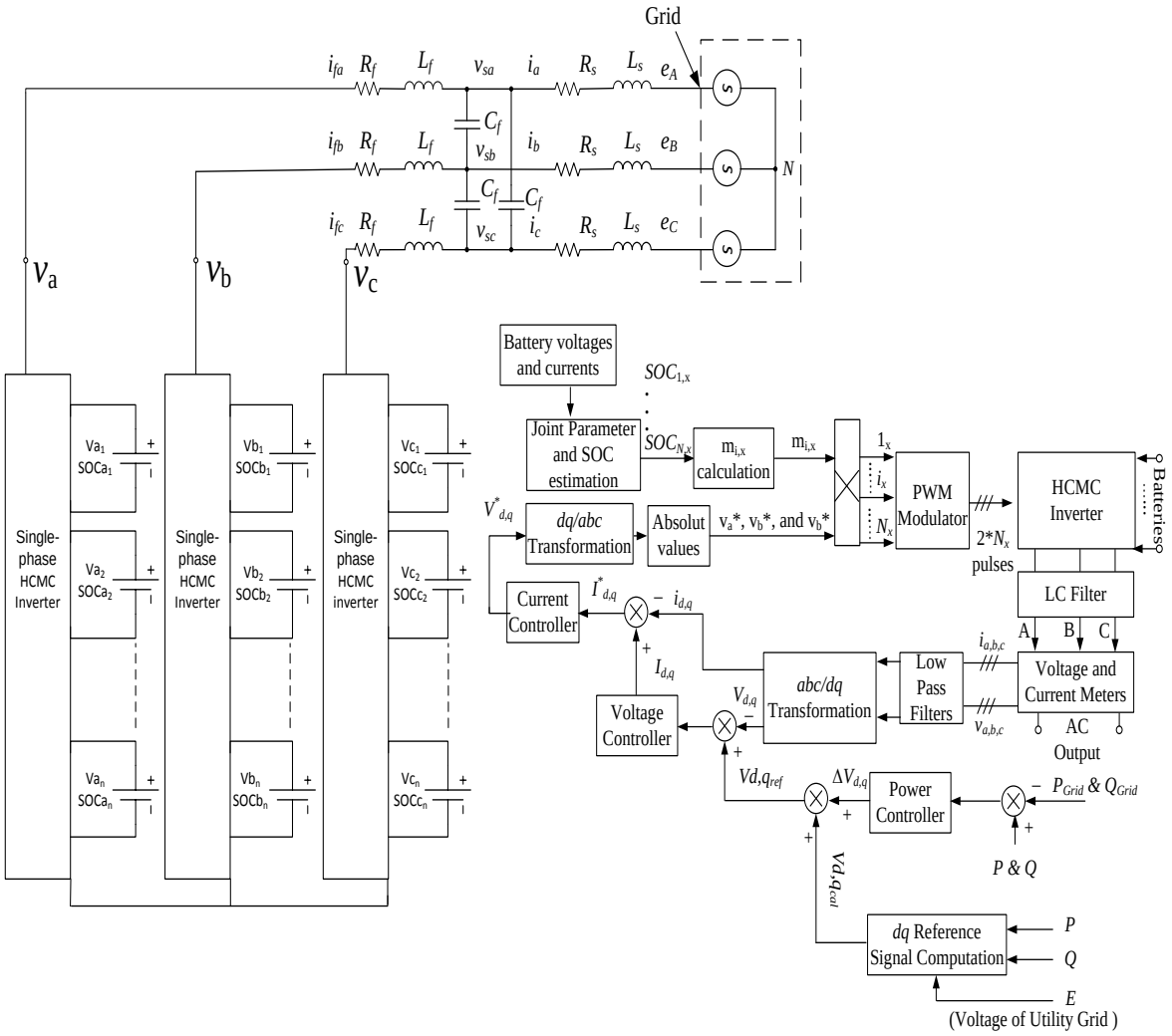


Fig. 34. Diagram of the overall BESS with power controller block.

The real and reactive powers delivered (under discharging) to or provided (under charging) by the grid are determined by the amplitude and angle of the output voltage of the cascaded inverter. The total output voltage phasor ($\vec{V} = V\angle\beta$) of the HCMC inverter is realized by the control of individual battery modules/cells. The charge and discharge of an individual battery module/cell (battery module i in phase x, x=a, b, c) is achieved through the control over the half-bridge converter connected to the module/cell ($E_{i,x}$). The charge

and discharge power can be regulated by controlling the modulation index $m_{i,x}$ (x=a, b, c) of the switching devices in each half-bridge converter, as shown in Fig. 31. For discharging control (delivering power back to the grid):

$$m_{i,x} = \frac{V_x}{E_{i,x}} \frac{SOC_{i,x}}{\sum_{i=1}^{n_x} SOC_{i,x}}, \ x = a, b, c \tag{3.12}$$

where V_x is the peak value of phase x of the inverter output voltage. $E_{i,x}$ is the terminal voltage of battery module i in phase x. n_x is the total number of battery modules in series for phase x.

In steady state, inverter output voltages v_a, v_b, and v_c in Fig. 34 should be the same for a balanced three-phase operation which can be done by controlling $m_{i,x}$ for each battery module on top of the uniform SOC management for all batteries in the strings. The β angle is used to regulate the overall power. For example, assuming that the phase angle of the grid voltage is 0°, a positive β will bring the cascaded multilevel inverter into discharge mode while negative β will set the converter at a charge mode. For charging control, the corresponding modulation index for battery module i in phase x can be obtained in a similar way:

$$m_{i,x} = \frac{V_x}{E_{i,x}} \frac{1-SOC_{i,x}}{\sum_{i=1}^{n_x}(1-SOC_{i,x})}, \ x = a, b, c \tag{3.13}$$

3.3 1.2kW/1.17kWh 208V Prototype System

3.3.1 Simulation Studies

In multilevel inverter topologies, the number of system components normally has a proportional relationship with the number of output voltage levels. Increased number of system components increases the size of inverter, weight, and cost, imposes a higher

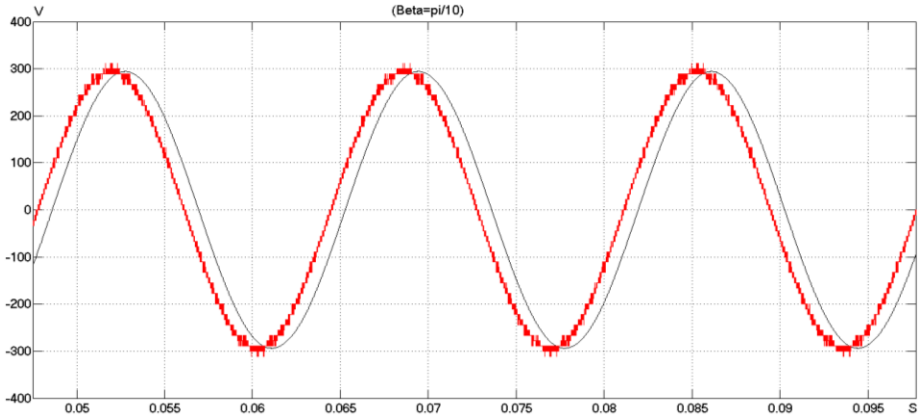
requirement of insulation, and also complicates the control. Moreover, these drawback factors will challenge the system reliability. Table 5 presents the number of components required to implement a nine-level inverter with different topologies including the proposed inverter. The proposed inverter achieves a 25% reduction in the number of system components required and uses only thirty-six switches compared with forty-eight switches used in a traditional cascaded H-bridge inverter.

Table 5 HCMC inverter: comparison of total component requirement for a nine-level inverter under different topologies.

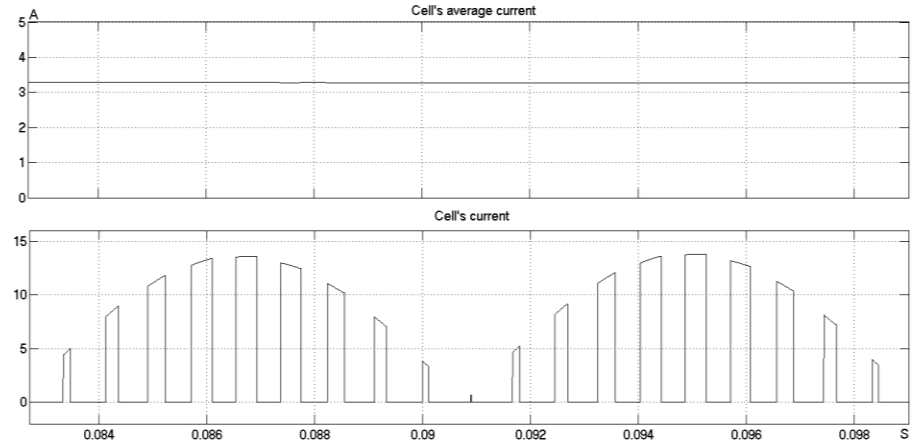
	Cascaded H-bridge [17]	New CMI inverter [72]	Sub-MI [33]	Proposed inverter
Transformers	0	0	2	0
Switches	48	36	36	36
Diodes	48	84	36	36
Total #	96	120	74	72
% of reduction	0%	-25%	22.9%	25%

To verify the effectiveness of the proposed converter, a battery system consisting of 48 battery modules (16 battery modules in each phase, i.e. n_x = 16) is simulated as shown in Fig. 31. Each battery module is an 11.1 V, 25W/24.42Wh unit, resulting in an overall system of 1.2kW/1.17kWh with an AC output voltage of 208 V (line-to-line voltage). Fig. 35 (a) shows the voltage waveforms of phase-A of both the grid and the HCMC inverter during a discharging cycle where the phase shift between them is set to $\pi/10$ (i.e., $\beta = \pi/10$). The carrier frequency is set at 600 Hz which is enough to improve the output waveforms. Based on (3.12), when the uniform SOC operation is achieved for every phase, the modulation index for each battery module in a phase string is calculated as:

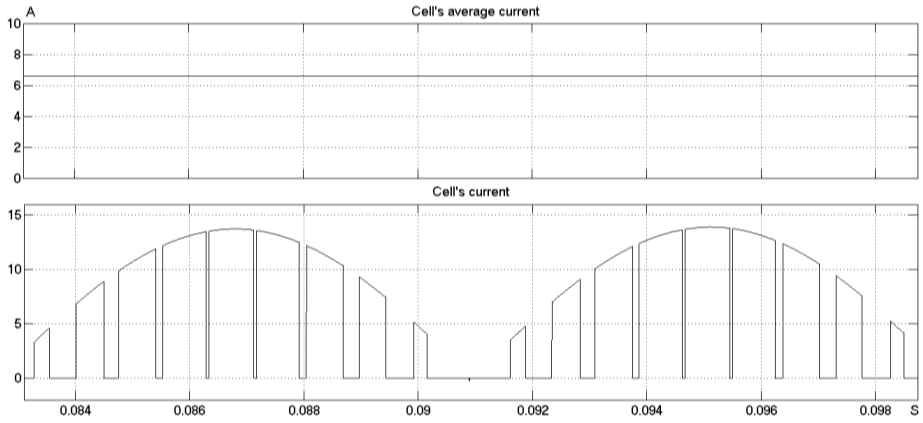
$$m_{i,x} = \frac{V_x}{E_{i,x}} \frac{SOC_{i,x}}{\sum_{i=1}^{N_x} SOC_{i,x}} = \frac{169.7}{11.1 \times 16} = 0.955$$



(a)



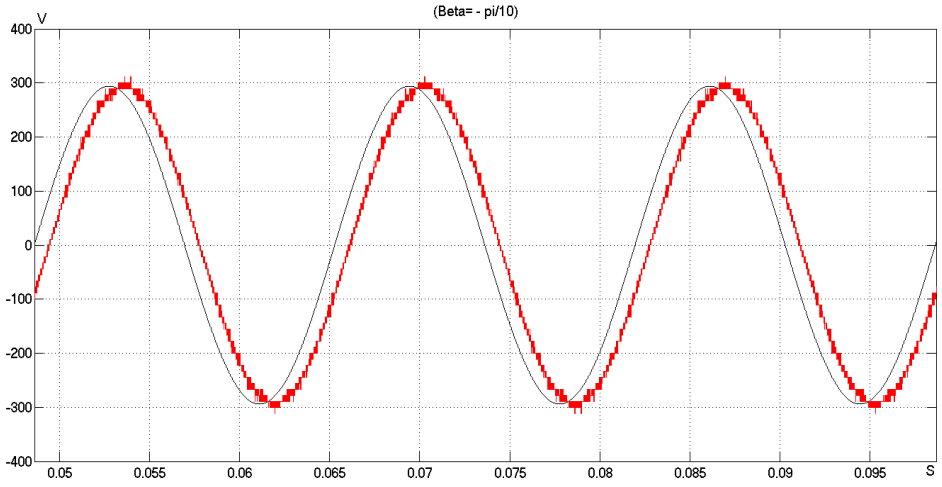
(b)



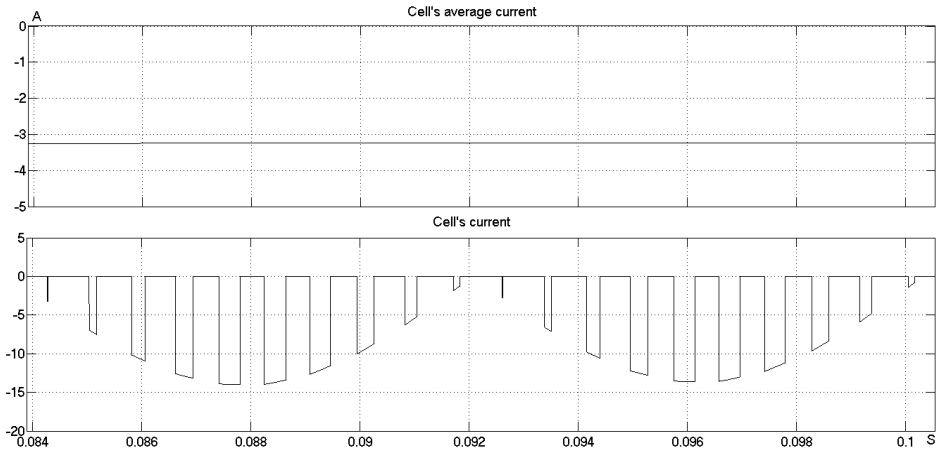
(c)

Fig. 35. Discharging process: (a) 33-level HCMC inverter and grid $V_{L\text{-}L}$ waveforms (fundamental frequency= 60Hz, and carrier frequency= 600Hz), (b) A module with a low SOC ($m_{i,x}$=0.5), (c) A module with a high SOC ($m_{i,x}$=0.97).

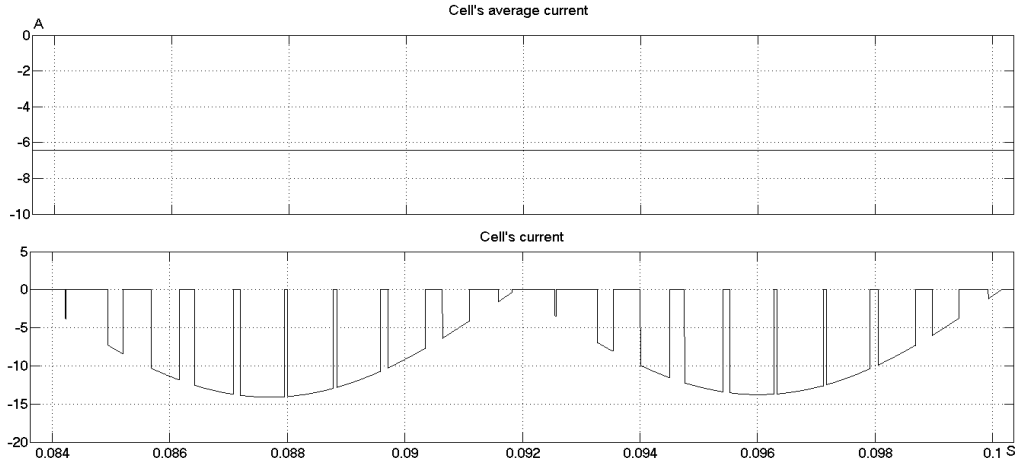
The current of a battery module with a low SOC is shown in Fig. 35 (b) while the current waveform of a battery module with a high SOC value is shown in Fig. 35 (c). It can be clearly seen that, by regulating individual $m_{i,x}$, the discharge power to each module can be different to achieve a uniform SOC operation. Fig. 36 shows the HCMC in a charging mode where β is set to be $-\pi/10$. In contrast to the discharging mode, a battery module with a higher SOC is charged less and a battery module with a lower SOC is charged at a higher power, as shown in Figs. 36 (b) and (c), respectively.



(a)



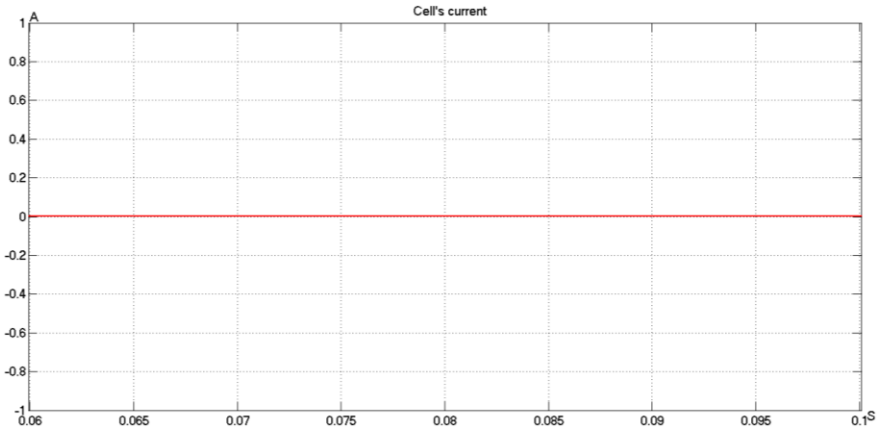
(b)



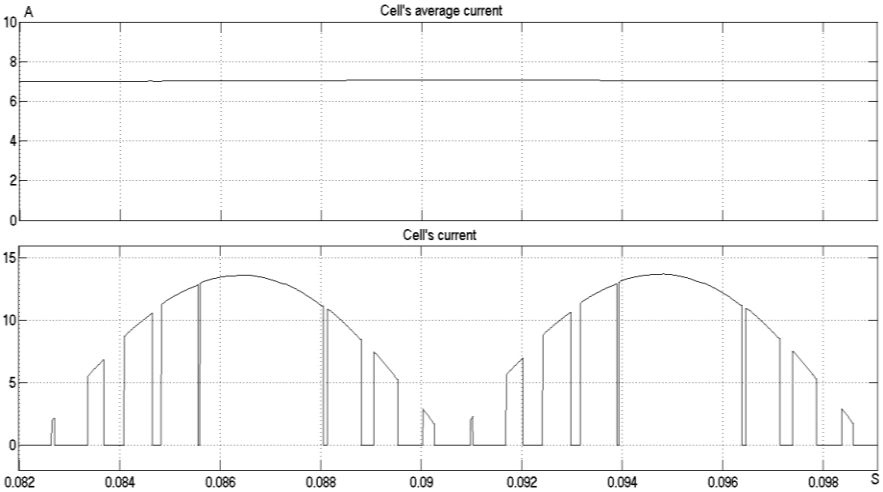
(c)

Fig. 36. Charging process: (a) 33-level HCMC inverter and grid $V_{L\text{-}L}$ waveforms (fundamental frequency= 60Hz, and carrier frequency= 600Hz), (b) A module with a higher SOC ($m_{i,x}$= 0.5), (c) A module with a lower SOC ($m_{i,x}$= 0.97).

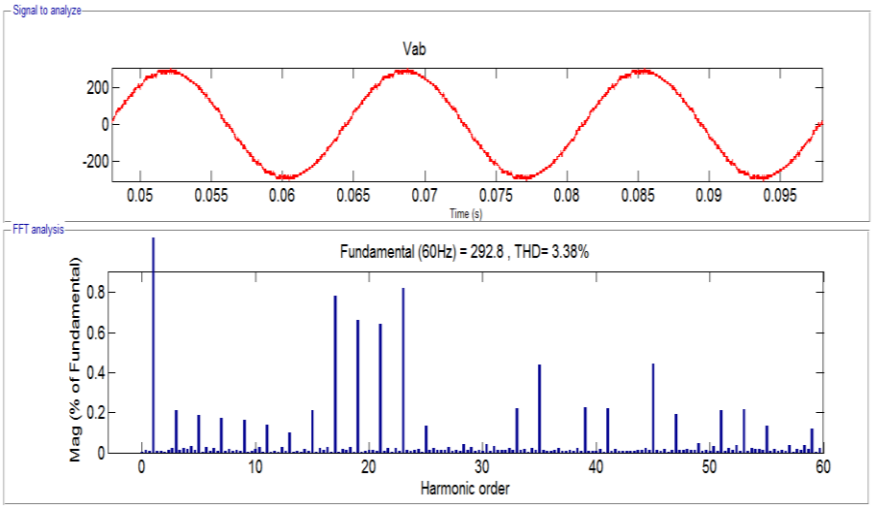
When one or more modules/cells need to be bypassed, the upper switching devices in the corresponding half-bridge converters should be turned off by applying zero modulation index, i.e., $m_{i,x}$= 0. As shown in Fig. 37 (a), a battery module in phase A is bypassed and its current becomes zero while the other modules still work properly. However, in this case, the overall phase output voltage with bypassed modules/cells will be reduced if no control action is done. In order to mitigate the voltage drop, the half-bridge converters of the other healthy in the same phase are controlled to generate a higher voltage with a higher modulation index. During this period of time, the whole system will be operated at a de-rated power and energy level. Moreover, the THD of the line to line voltages are affected, as shown in Fig. 37 (c), (d), and (e). In this case, the affected voltages by the bypassed battery module in phase A are V_{ab} and V_{ac} with a higher THD of 3.4%, compared a THD of 2.67% for V_{bc}.


Cell's current
A
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
0.1
S

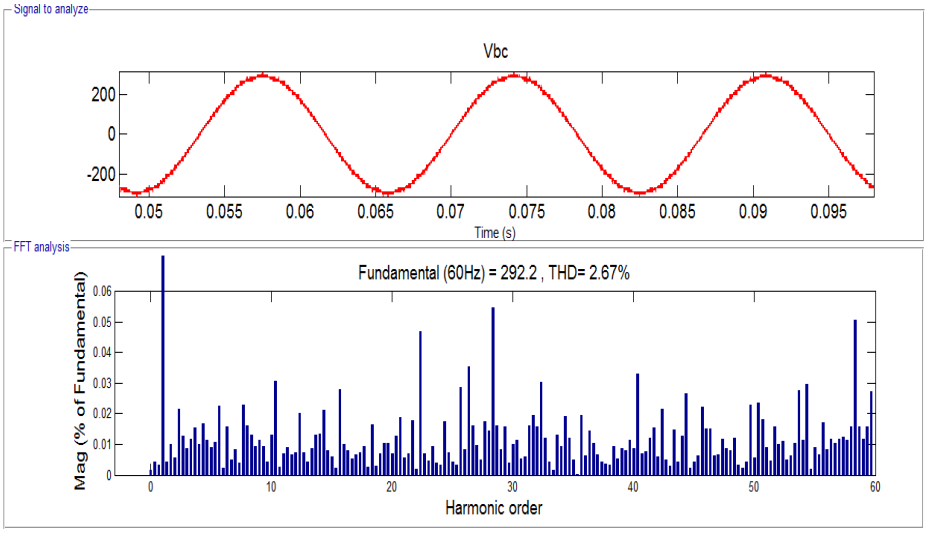
(a)


Cell's average current
A
10
8
6
4
2
0
Cell's current
15
10
5
0
0.082
0.084
0.086
0.088
0.09
0.092
0.094
0.096
0.098
S

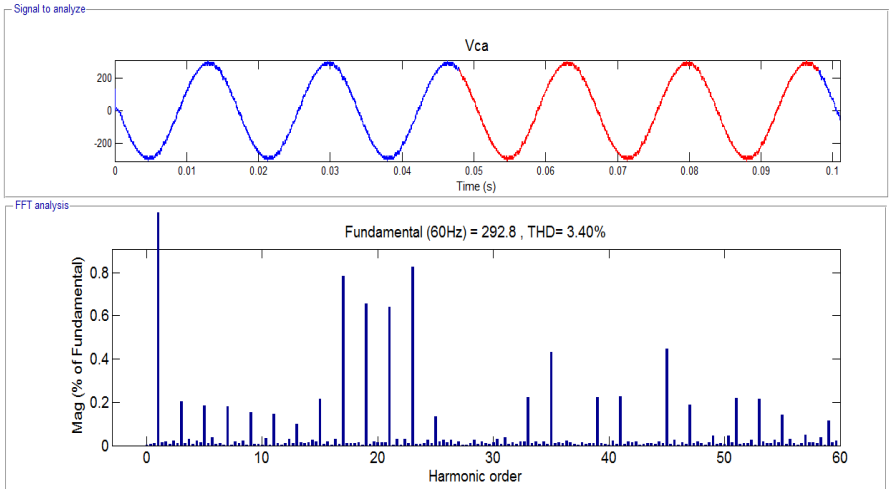
(b)


Signal to analyze
Vab
200
0
-200
0.05
0.055
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
Time (s)
FFT analysis
Fundamental (60Hz) = 292.8 , THD= 3.38%
Mag (% of Fundamental)
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
Harmonic order

(c)



(d)

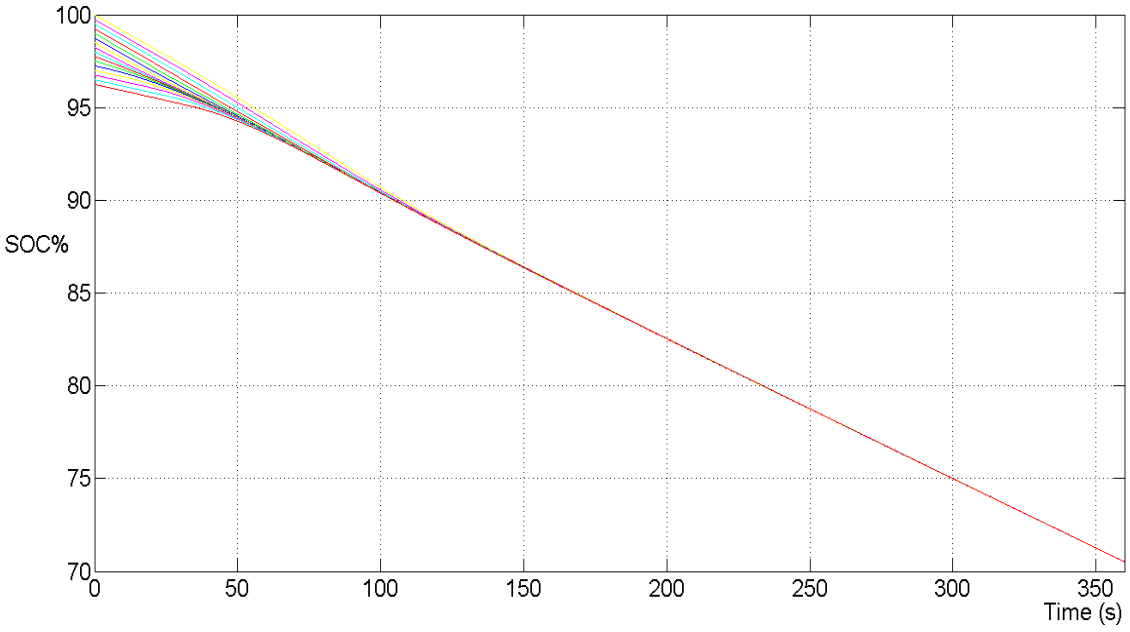


(e)

Fig. 37. Bypassing a battery module: (a) Current of bypassed cell ($m_{i,x}$= 0), (b) Current of other healthy battery cells ($m_{i,x}$> 1), (c), (d), (e) are the line to line output voltage waveforms with their THD values after bypassing a battery from phase A.

To verify the performance of the proposed SOC balancing scheme, a BESS of 48 battery packs is simulated as shown in Fig. 34. The proposed control strategy can not only realize the real and reactive power flow control, but also uniform the SOC of batteries in the system. All battery modules charge/discharge with their own individual SOC initial conditions. The batteries with higher SOCs will be controlled to share more power delivery in the discharging mode while the batteries with lower SOCs will be controlled to be charged

with more power in the charging mode. Also, the string-average (or the phase-average) SOC is different among the three battery strings (i.e., in the discharging process: $SOC_a > SOC_b > SOC_c$ while in charging mode $SOC_a < SOC_b < SOC_c$) which will be discussed in Chapter 4. This chapter demonstrates uniform SOC battery modules among individual battery string. During discharging process, the SOC initial conditions of battery modules vary in phase A from 100% to 96.25% (i,e, 0.25% between any two adjacent batteries). In phases B, and C, the initial SOCs for the first batteries are 98%, and 96% respectively while the SOCs of the other modules vary in the range of (95.75-92.25) % and (91.75-88.25) %, respectively. However, based on (3.12), the variations of SOCs between batteries in a string can be balanced by the proposed control method where the SOC is taken into account. The module with a higher SOC is discharged more. Therefore, the SOC equalization or the SOC variation elimination is achieved as shown in Fig. 38.



(a)

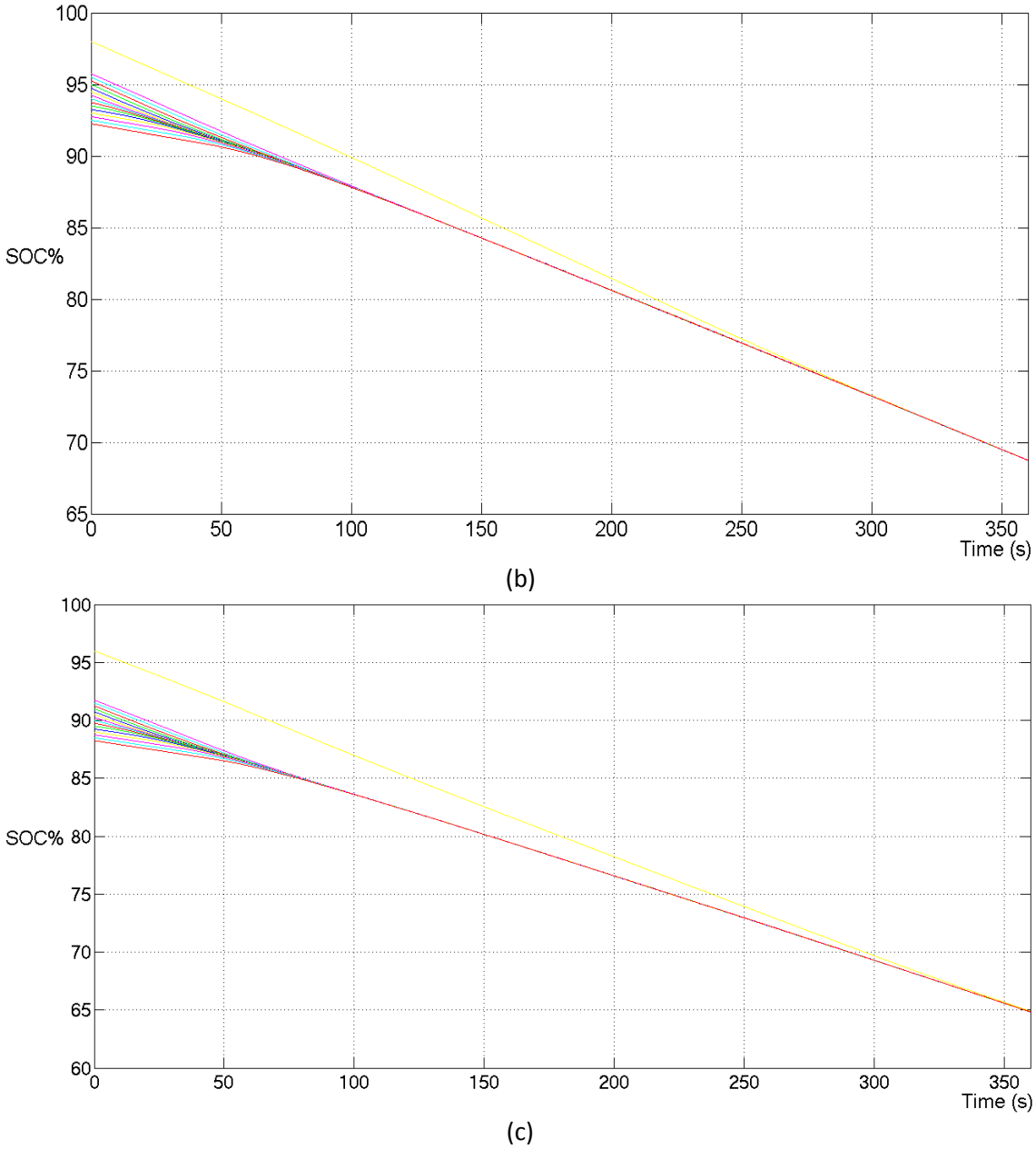
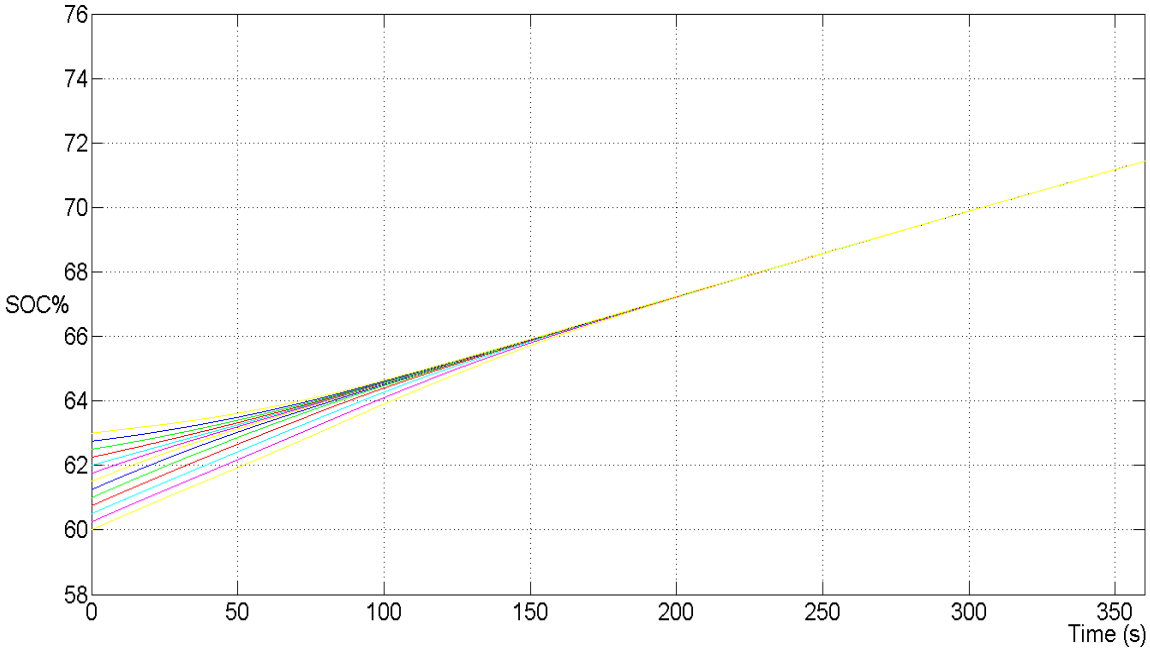


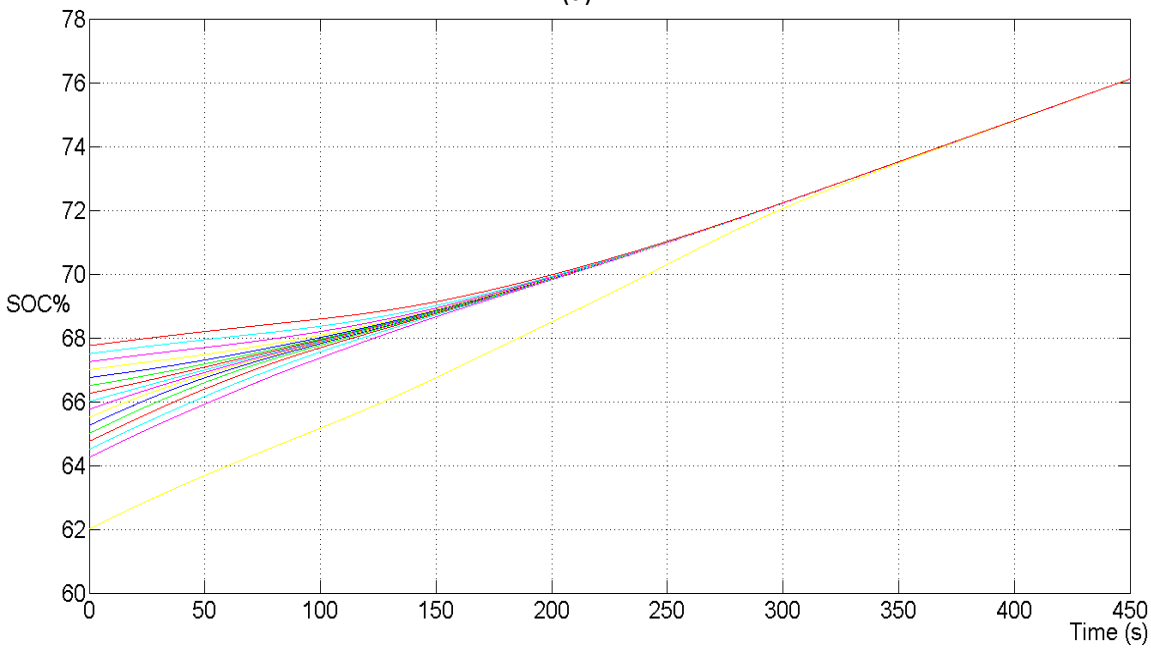
Fig. 38. SOC balancing of the battery modules during the discharging process: (a) Phase A, (b) Phase B, and (c) Phase C.

In the charging process, Fig. 39 shows the convergence to the uniform SOC. The initial SOC values of the battery modules vary in phase A from 60% to 63.75%. The first batteries in phases B and C start from 62% and 64% respectively and the SOC variations of the rest battery modules are (64.25- 67.75) %, and (68.25–71.75)%, respectively. Based on

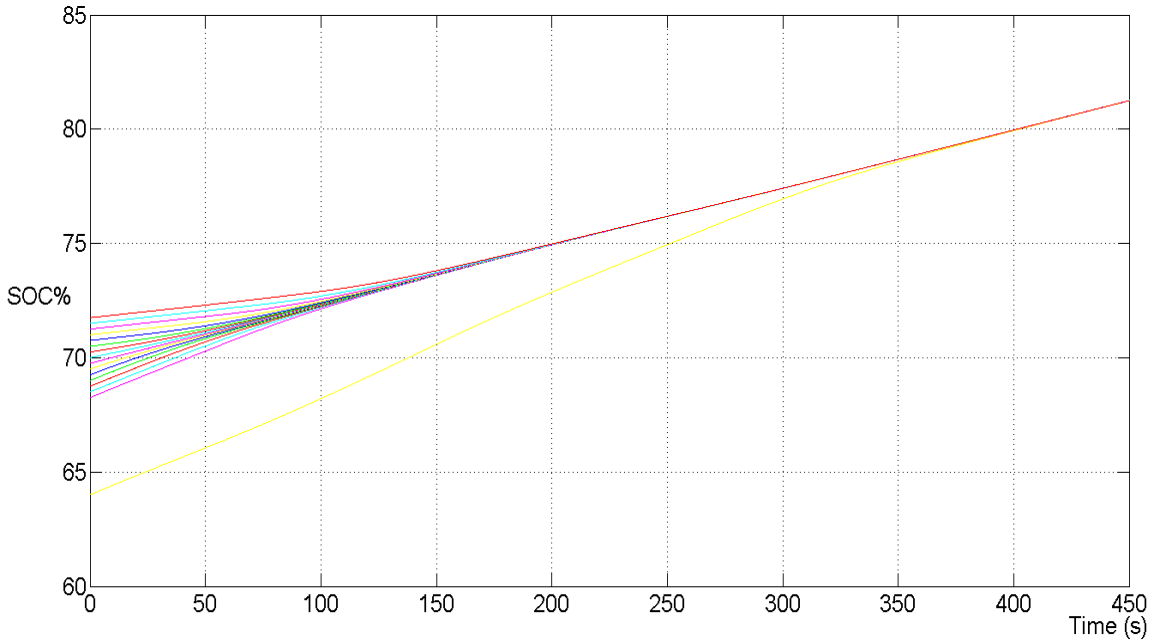
(3.13), a battery module with a higher SOC is charged less and a battery module with a lower SOC is charged at a higher power. Hence, a uniform SOC distribution among the batteries in the system can be eventually achieved.



(a)



(b)



(c)

Fig. 39. SOC balancing of modules during charging process: (a) phase A, (b) phase B, and (c) phase C.

3.3.2 Circuit Implementation

3.3.2.1 Inverter Design

The first work to be done before implementation is to determine the minimum dc-link voltage requirement. The lowest dc-link value to realize an output phase-voltage using a sinusoidal PWM technique is given as follows:

$$V_{dc,min} = V_{ph} * \sqrt{2} \tag{3.14}$$

In real applications, the inverter circuit under transient conditions must be taken in account by selecting an appropriate margin of reserve-voltage to guarantee the proper operation [139, 140]. Also, we need to consider voltage drop on battery cells during charge/discharge processes. Therefore, 10% of the minimum dc-link as a margin can be considered for compensating voltage drops in the BESS. Another 10% of the minimum dc-

link to control switching devices without causing over-modulation which occurs when the modulation index m is greater than unity and hence dc-link given by:

$$V_{dc} = 1.2 * V_{dc,min} \tag{3.15}$$

As can be seen from Fig. 31, the topology is a hybrid combination of both H-bridge and half-bridge converters that can be cascaded at two hierarchical levels, i.e. the H-bridge level and half-bridge level. Therefore, we have low and high rated voltage devices: the half-bridge converters work at the battery module rated voltage (low voltage side) while the H-bridge converters work at a voltage level of certain number of cascaded half-bridge converters. The number of converter cells per phase in our inverter for both hierarchical levels can be determined as:

1. H-bridge inverter.

$$Y \geq \frac{V_{dc,inverter}(1+x)}{V_{H-bridge}} \tag{5.10}$$

2. Half-bridge converter

$$y \geq \frac{V_{dc,H-bridge}(1+x)}{V_{half-bridge}} \tag{5.11}$$

where $V_{dc,inverter}$, $V_{dc,H-bridge}$, and $V_{half-bridge}$ are the voltage of single-phase, H-bridge, and battery module dc-links, respectively. Safety factor x takes into account the stresses of the switching devices produced by stray inductances on semiconductor switches [140]. The values Y and y are the number of the H-bridge power inverters and the half-bridge modules/cells per-phase, respectively. However, no straightforward guidelines that can be applied for all applications and hence the rated values have to be selected case by case [139]. Nevertheless, for a direct grid connection, 2.5 kV IGBT is recommended for 1200V

applications as a maximum rated voltage and 6.5 kV IGBT is recommended for a maximum rated voltage of 3600V [141]. Therefore, x can be any value depends on the actual applications and grid integration requirements. In this work, safety factor x is considered to be 0.5 because the 1.2kW/1.17kWh energy storage system will be connected to a low voltage network (i.e. 208V). Table 6 shows the circuit specification of the proposed system.

Table 6 Circuit specification of 1.2kW/1.17kWh 208V system.

System DC link	170V	
Battery voltage	11.1V	
Max. DC link	177.6V	
Modulation index	m= 0.955	
3rd harmonic injection	New max. DC link = 206V	
Safety margin	36V, 20%	
H-bridge	# of semiconductor switches	48
	dc link	44.4V
	safety factor	0.5
	$V_{H\text{-}bridge}$	≥ 66.6V
	$I_{H\text{-}bridge}$	≥ 8.8 (4*$I_{Battery}$) A
Half-bridge	# of semiconductor switches	96
	dc link	11.1V
	safety factor	0.5
	$V_{half\text{-}bridge}$	≥ 17V
	$I_{half\text{-}bridge}$	≥ 8.8 (4*$I_{Battery}$) A
Batteries	Li-ion 2200mAh	
Switches	H-bridge	N-MOSFET 100V 24A 2.95mΩ
	Half-bridge	N-MOSFET 30V 30A 1.8mΩ

3.3.2.2 Experimental Results

To verify the proposed modulation strategies, Fig. 40 shows the three-phase 33-level inverter prototype. The CPS-PWM is implemented based on a digital signal processing (DSP) TMS320F28335 control board. All dc input sources are lithium-ion battery modules with 11.1V rating voltage and 2.2Ah (24.42Wh) capacity. The switching frequency and line frequency of the inverter is 480Hz and 60Hz, respectively. The load is a pure resistor of 47 ohm. In each half-bridge circuit, the device ISL9N315AD3ST with 30V and 30A rating is selected while in full-bridge circuit, the device NCE0128D with 100V and 28A rating is selected. The gate driver is implemented by the device HCPL3120.

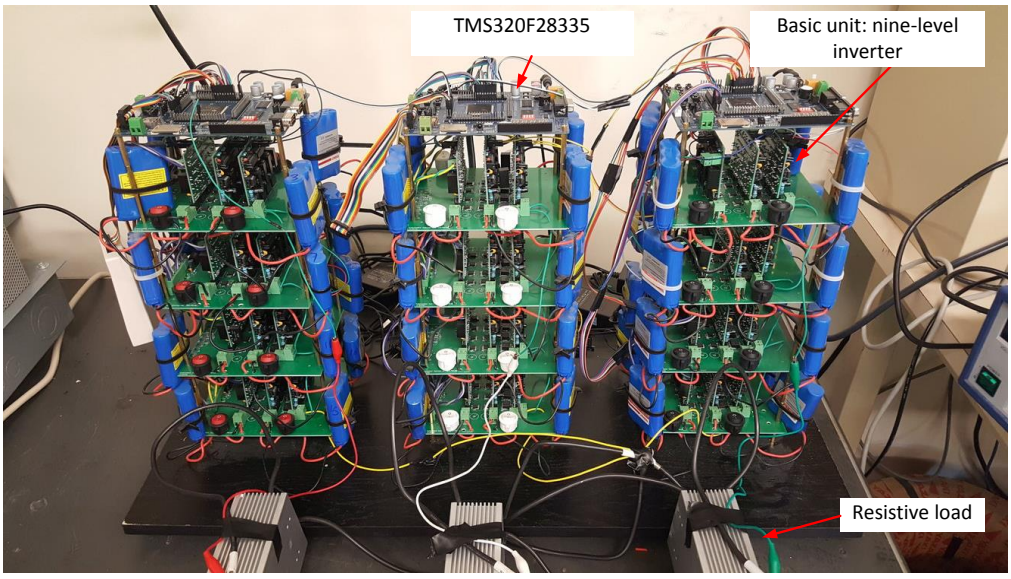


Fig. 40. The experimental prototype.

With a DSP based control board, ePWM is usually utilized to implement the modulation scheme for a converter. However, the number of ePWM in the DSP board is limited. So, some other digital control boards such as CPLD and FPGA are needed, which increases design cost. In this work, this limit is addressed by the main program in Fig. 41, where an interrupt timer is used instead of ePWM. It can be seen from Fig. 41 that sixteen

triangular carriers are produced by an interrupt function Cpu_Timer0_Interrupt (). The logic comparator operation can be easily implemented with some simple logic judgement operations such as addition and subtraction. According to the key code in Fig. 41, the obtained S_i (i=0, 1…,15) is a logic value (0 or 1). Therefore, general purpose input output (GPIO) terminals can be utilized to output switching signals according to switching logics. The key configurations for GPIO terminals are given as follows:

```
if (S_i)
   GpioDataRegs.GPASET.bit.GPIOi = 1;    (i=0, 1…15)
else
   GpioDataRegs.GPACLEAR.bit.GPIOi = 1;
```

If S_i is the logic value 1, the corresponding output GPIO terminal is set high; otherwise, it is set low.

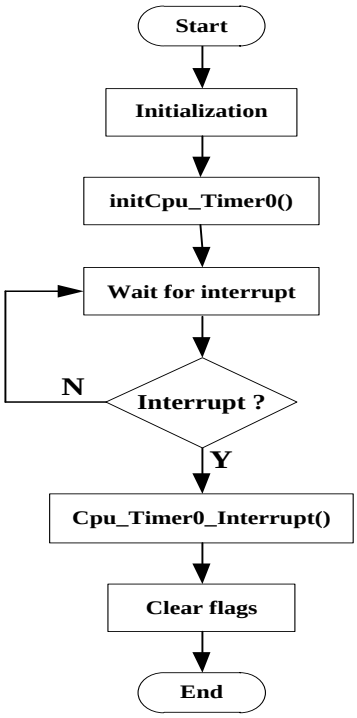


Fig. 41. Flow chart of the main program.

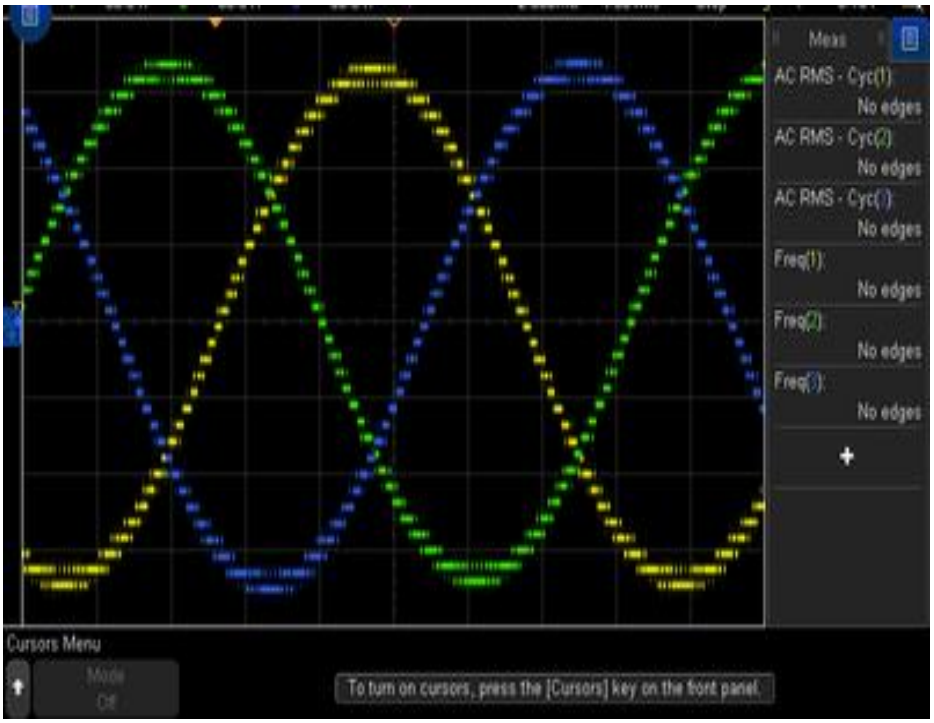


Fig. 42. Experimental voltage waveforms of 33-level HCMC inverter.

Fig. 42 shows experimental output voltages of the HCMC inverter where each phase has thirty-three voltage steps. The SOCs of battery modules are unknown, but the terminal voltages of battery modules/cells are approximately linear-proportional to their SOCs. Therefore, the control strategy of uniform SOC is based on the open-circuit voltage method which can reflect capacity of battery modules. Fig. 43 shows terminal voltages of battery string of sixteen modules with different initial values of output voltages. Based on (3.12), during discharge process, the open circuit voltages can be uniformed by applying the proposed PWM scheme where measurements are taken every four mints. The modulation indices were changed every four mints based on the new values of open circuit voltages. The module with a higher terminal voltage is discharged more. Thus, the SOC equalization or the SOC variation elimination is achieved.

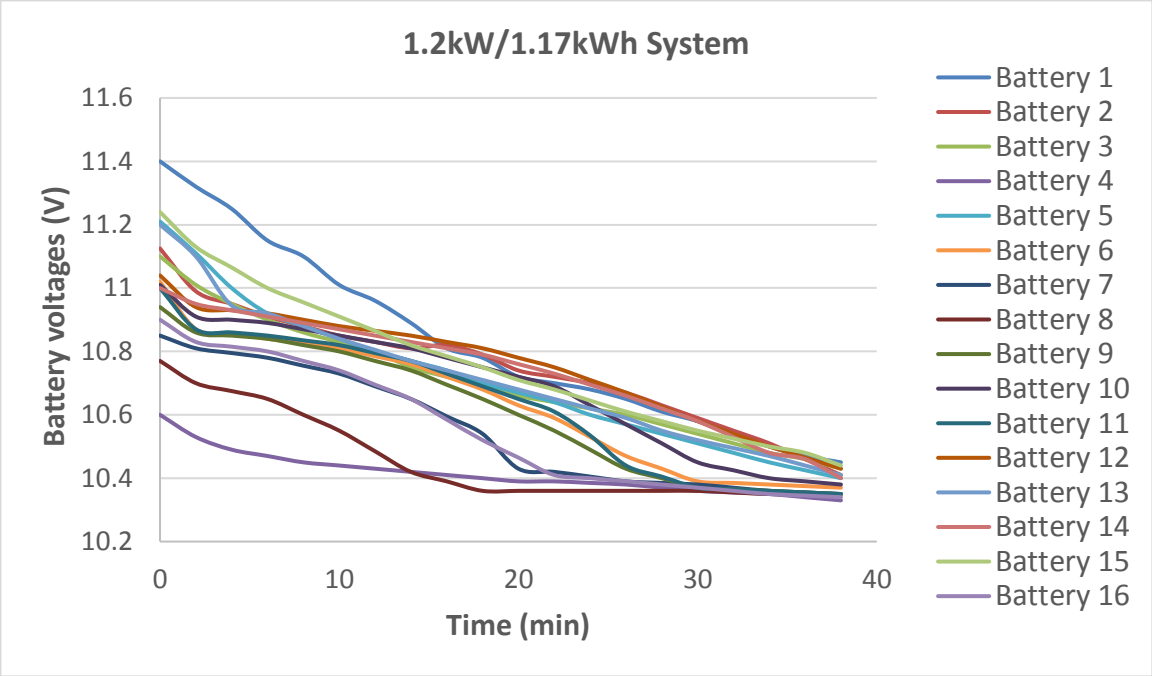


Fig. 43. Terminal voltage uniform result during discharge process.

CHAPTER 4 IMPROVED HCMC WITH PHASE-TO-PHASE SOC BALANCING CAPABILITY

In a three-phase Cascaded Multilevel Inverter (CMI) based battery system, the SOC balancing can be achieved within individual phases [111]. On the other hand, it is challenging to achieve SOC balancing among all the phases for a uniform SOC operation of the entire system since the battery modules/cells in each phase are managed separately in CMIs. A neutral point voltage injection method was proposed in [142], [143] for three-phase SOC balancing. However, this will cause asymmetrical terminal quantities of the converter [143]. A negative-sequence voltage injection method was presented in [144] for three-phase energy balancing. Similar to the method in [143], the negative-sequence voltage injection produces a negative-sequence current, resulting in unbalanced three-phase operations in terms of electrical quantities. A new DC-link voltage optimization method is proposed in [145]. Like previous mention methodologies, the BESS is charge/discharge under unbalance operation to balance average SOC among phases.

This chapter presents a new three-phase SOC equalizing circuit, called six-switch balancing circuit, which can be used to realize uniform SOC operation for full utilization of the battery capacity in the three-phase BESS. A sinusoidal PWM modulation scheme is proposed to control power transferring between phases in a cascaded multilevel inverter. Simulation results have been carried out to verify the performance of the proposed circuit for uniform three-phase SOC balancing.

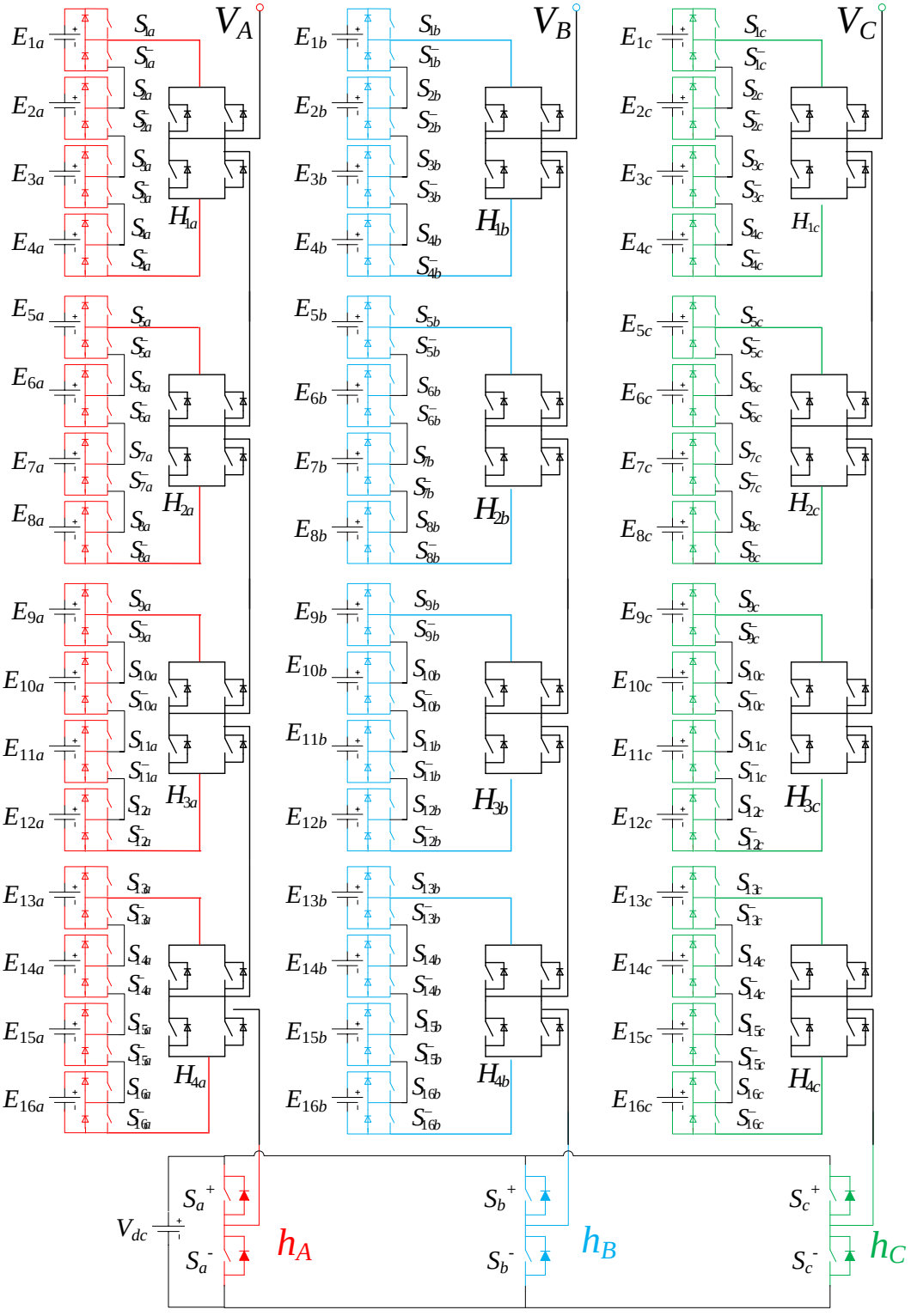


Fig. 44. Thirty-three-level HCMC inverter with SSBC.

4.1 Circuit Topology

For a large-scale battery system consisting of separate battery packs for individual phases, the battery packs in different phases are more likely to have different capacities. As a result, even if the uniform SOC can be maintained for the batteries within each phase [111], there can be substantial SOC differences among phases, which decrease the whole system's battery utilization and the system reliability. Therefore, three-phase uniform SOC operation is important to utilize the full capacity of the whole battery system. In the following proposed circuit, a uniform three-phase balanced SOC operation is achieved for the whole system. Although the proposed phase-to-phase balancing circuit also works for other types of CMIs, the focus in this chapter is given to a hierarchical cascaded multilevel converter (HCMC) that we have developed [111], as discussed in Chapter 3.

The six-switch balancing circuit (SSBC) is introduced in this section. It is at the bottom level of the cascaded converter and provides a path for power transfer between the phases as shown in Fig. 44. A common battery module (i.e., a common DC source) is used in the three-phase SSBC. In addition to the capability of transferring power between phases, the proposed SOC balancing circuit can be used as a three-phase inverter and work as a part of the HCMC to increase the system power/energy ability if needed.

The proposed structure involves two SOC balancing levels (i.e., phase and phase-to-phase SOC balancing levels) and hence utilizes the full capacity of BESS. To achieve the first level, the HCMC is used to control power of individual battery modules/cells. The circuit topology and control strategy have been discussed in detail in Chapter 3. The three-phase circuit of SSBC can be realized by adding three half-bridge converters (i.e., one half-

bridge per phase) that are connected to the same common dc link, as shown in Fig. 44. The DC source can be charged/discharged through the upper switching devices (i.e., S_a^+, S_b^+, and S_c^+) in the half-bridge converters.

4.2 Phase-to-phase SOC Balancing

The half-bridge converters h_A, h_B, and h_C in Fig. 44 are controlled based on the average SOC value of the batteries in each phase which can be given by

$$SOC_x = \frac{1}{N_x}\sum_{i=1}^{N_x} SOC_{x_i} \qquad x = a, b, c \tag{4.1}$$

where N_x is the total number of battery modules/cells per phase and the average SOC for the whole system can be expressed as

$$\overline{SOC} = \frac{1}{3}(SOC_a + SOC_b + SOC_c) \tag{4.2}$$

The power of charge/discharge processes can be regulated by controlling the modulation indices k_a ,k_b, and k_c of the upper switching devices S_a^+, S_b^+, and S_c^+, respectively. The modulation indices for the three half-bridge converters in the SSBC can be determined as:

$$k_x = \frac{\overline{SOC} - SOC_x}{\Delta SOC_{max}}, x = a, b, c \tag{4.3}$$

Where $\Delta SOC_{max} = \max_x(|SOC_x - \overline{SOC}|),\ x = a, b, c$. It should be noted that the batteries in each phase are managed by the HCMC to operate at its uniform SOC, i.e., SOC_x, $x=a, b, c$, as previously discussed.

As indicated in (4.3), the modulation index k_x for each phase leg in the SSBC can be negative. When k_x is negative, the reference voltage waveform for S_x^+ in the corresponding

half-bridge converter (i.e., phase *x* in the SSBC) is 180° out of phase compared to the reference voltage for phase *x* in the main HCMC. On the other hand, if k_x is positive, then the reference voltage waveform for S_x^+ in the corresponding half-bridge converter (i.e., phase *x* in the SSBC) is in phase with the reference voltage for phase *x* in the main HCMC. For example, consider a case that the main battery system is under discharge, and $SOC_a > SOC_c > SOC_b$ and $SOC_c = \overline{SOC}$. In this case, $k_a = -1$, $k_b = 1$, and $k_c = 0$. The energy will be transferred from phase A to phase B until a uniform SOC is achieved for all the three phases.

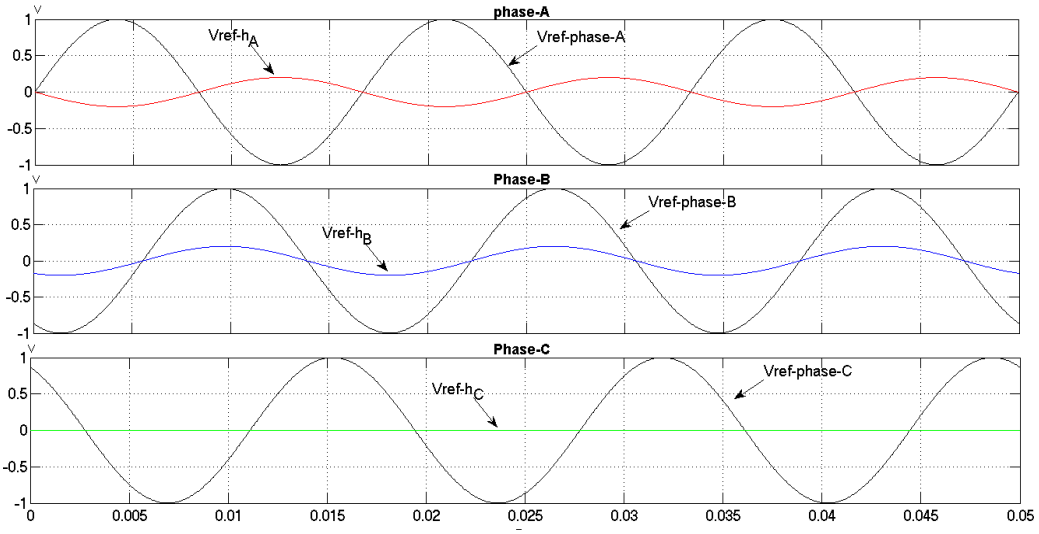


Fig. 45. Three-phase reference voltage waveforms of the main CMI and the SSBC when $k_a = -1$, $k_b = 1$, and $k_c = 0$.

Fig. 45 shows the reference voltage waveforms of the SSBC. It can be clearly seen from the figure that the reference voltage waveform for S_a^+ in the half-bridge converter of h_A is 180° out of phase from the reference voltage waveform of phase A in the main HCMC. The reference voltage waveform for S_b^+ in the half-bridge converter of h_B is in phase with the reference voltage waveform of phase B in the HCMC. As a result, in addition to the regular phase power, the batteries in phase A of the main HCMC are to be discharged more by also charging the battery in the SSBC. On the other hand, the batteries in phase B of the

main HCMC are to be discharged less since the battery in the SSBC is in phase with it to provide support to the phase. Note that the battery in the SSBC does not store or discharge energy in a cycle. It basically transfers the energy among phases in the main system. This is actually guaranteed by the control law given in (4.3), which ensures that

$$\sum_x k_x = 0, \quad x = a, b, c \tag{4.4}$$

The instantaneous charge/discharge power of the battery in the SSBC is given by

$$p_{dc}(t) = (S_a(t) \times I + S_b(t) \times I + S_c(t) \times I) \times V_{dc} \tag{4.5}$$

where S_a, S_b , and S_c are the switch states of upper switches S_a^+, S_b^+, and S_c^+, respectively. V_{dc} and I are the dc source voltage and the current of each half-bridge converter in the SSBC, respectively. Thus, the average power of the SSBC is:

$$\bar{P}_{dc} = (k_a \times I + k_b \times I + k_c \times I) \times V_{dc} = 0 \tag{4.6}$$

4.3 Simulation Results

To verify the effectiveness of the proposed balancing circuit, a battery system consisting of 48 battery modules (16 battery modules in each phase, i.e. N_x= 16) with SSBC is simulated, as shown in Fig. 46. Fig. 47 shows the voltage waveforms of phase A of both the grid and the HCMC inverter during a discharging cycle where the phase shift between them is set to π/10 (i.e., β= π/10). The carrier frequency is set at 360 Hz, which is enough to improve the output waveforms.

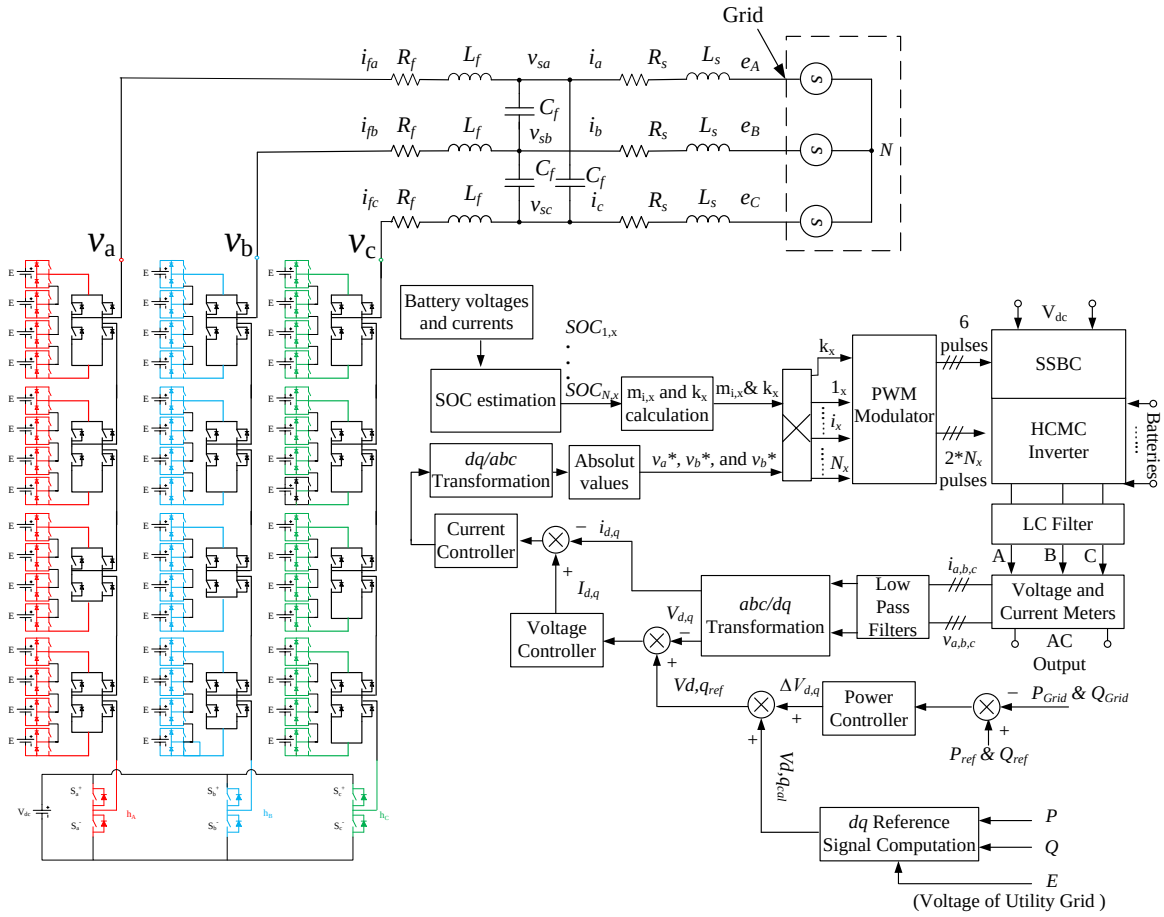


Fig. 46. Diagram of the overall system with power controller block.

As previously discussed, the batteries in each phase can be managed to achieve a uniform SOC operation based on the control law given in (3.12) and (3.13). However, due to the battery capacity differences in the three phases, the three phases can have different SOC values. Without loss of generality, consider a case of SOC_a = 0.98, SOC_b = 0.92, and SOC_c =0.95. Fig. 48 shows the voltage waveforms of the system connecting to the SSBC circuit with a DC voltage =14.8 V. To bring the system back into the balance mode, both $m_{i,a}$, and $m_{i,b}$ should be changed as shown in Fig. 48.

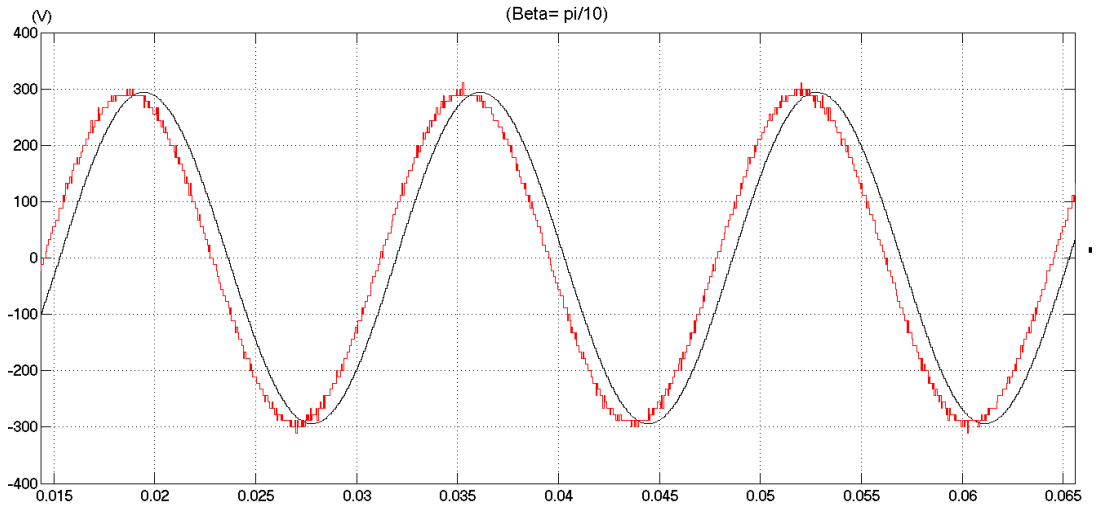


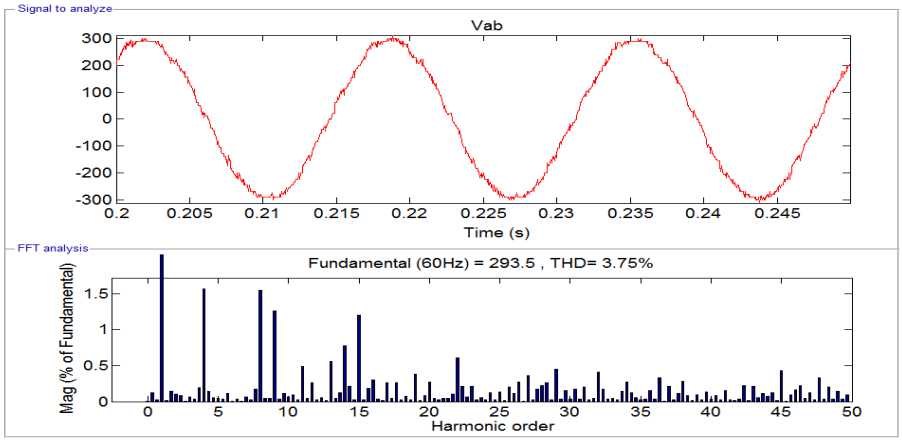
Fig. 47. Thirty-three level HCMC inverter and grid $V_{L\text{-}L}$ waveforms (m_i=0.95, fundamental frequency= 60Hz, and carrier frequency= 360 Hz).

According to the control strategy discussed in Section 4.2 for the SSBC, the modulation indices are $k_a = -1$, $k_b = 1$, and $k_c = 0$. Since phase A in the SSBC is 180 degree out of phase with respect to phase A in the main HCMC, the modulation index of the batteries in the phase needs to be increased to compensate the voltage difference introduced by the SSBC. It actually discharges phase A in the main HCMC and charges the battery in the SSBC. Based on (3.12), the new modulation index for phase A in the HCMC now is:

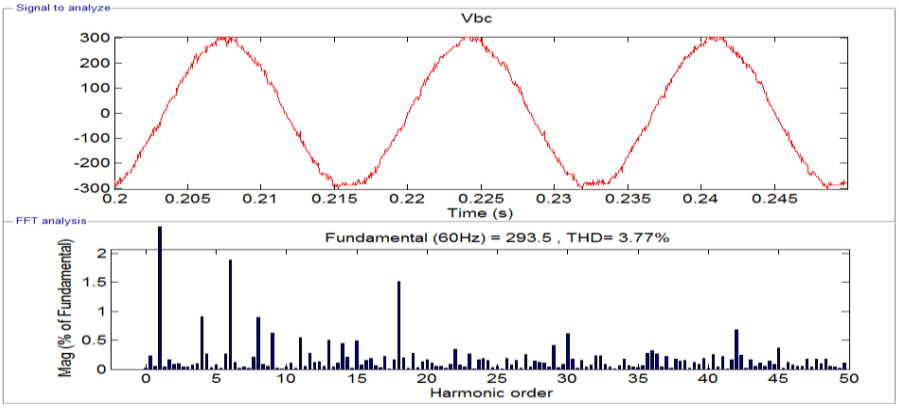
$$m_{i,a} = \frac{V_{sm,a}}{E_{i,a}} \frac{SOC_{i,a}}{\sum_{i=1}^{N_a} SOC_{i,a}} = \frac{169.7 - (-14.8/2)}{11.1 \times 16} = 1.0$$

Similarly, we can obtain the modulation index for phase B in the HCMC as $m_{i,b} =$ 0.9. The modulation index for phase C is the same as before since there is no change. Fig. 48 shows the output of the overall converter with the SSBC integrated. The batteries in phase A in the main HCMC is controlled to discharge more since it has the highest SOC value while the batteries in phase B in the main HCMC is controlled to discharge less. The batteries in phase-C in the main HCMC are controlled to discharge as before. In this way, the energy

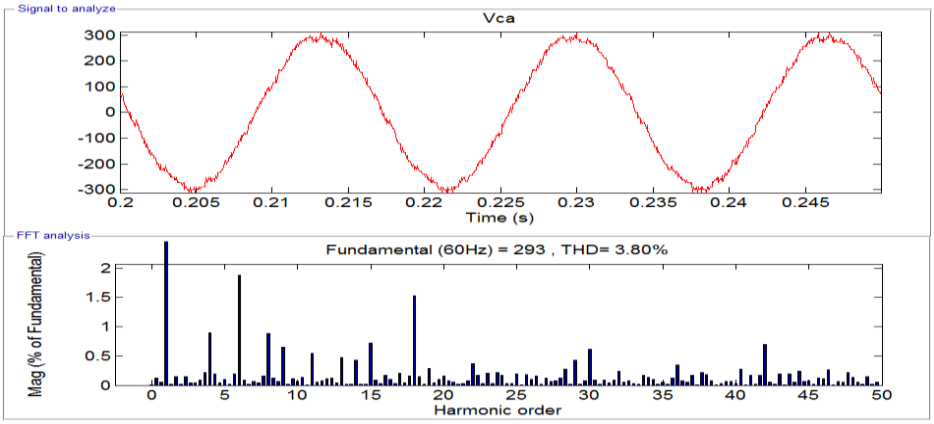
is transferred from phase A to phase B via the SSBC, resulting in a uniform SOC for all the three phases. In this case, the battery in the SSBC does not store or discharge any energy as shown in Fig. 49. If it delivers a given amount of energy in the first half period, it will absorb the same amount of energy in the next half cycle. Fig. 50 shows uniform process of SOC among three-phase battery strings during discharging mode. The initial SOC difference between battery stings in phases A and B is 6% that can be eliminated by power transferred between phases. Hence, a uniform SOC distribution among the battery strings in the system can be eventually achieved.



(a)



(b)



(c)

Fig. 48. SSBC connected to the HCMC system: (a), (b), (c) are L-L voltage waveforms with their THD ($m_{i,a}$=1, $m_{i,b}$ =0.9, $m_{i,c}$ =0.95, fundamental frequency= 60Hz, and carrier frequency= 360 Hz).

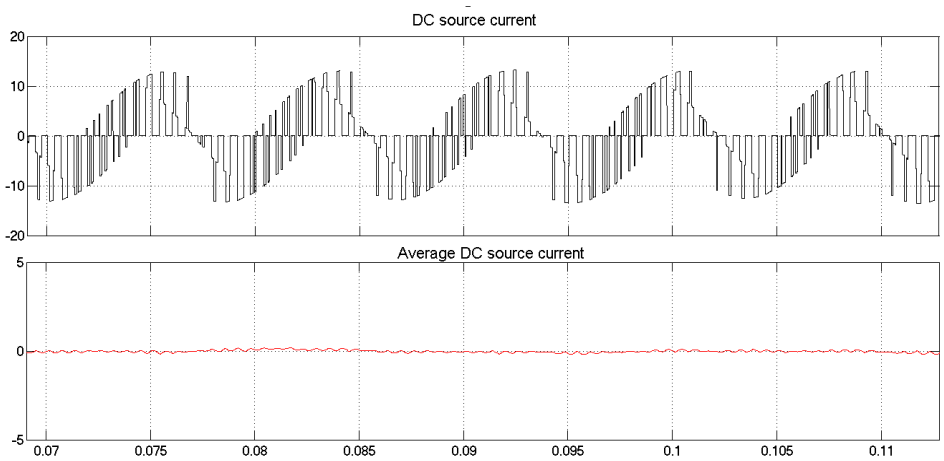


Fig. 49. DC source current of the SSBC circuit.

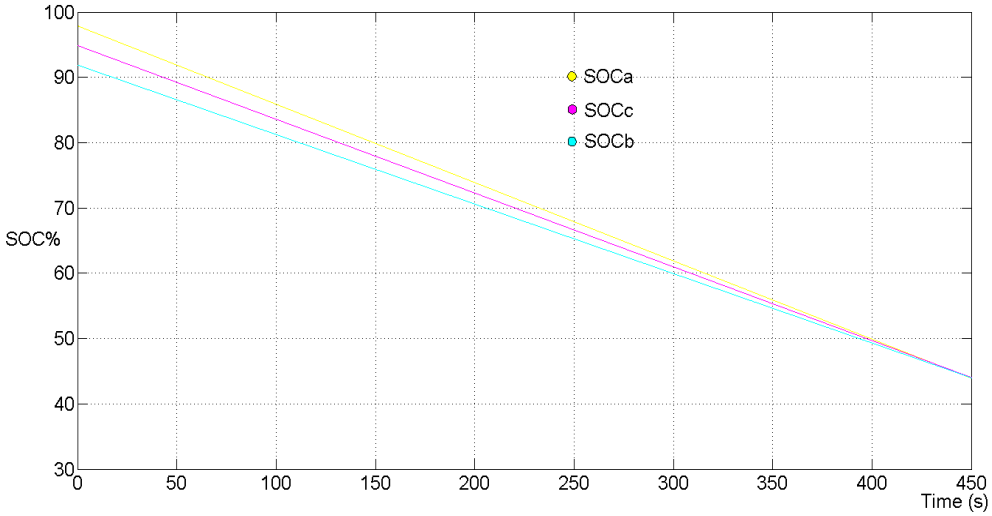


Fig. 50. SOC balancing of battery strings during the discharging process.

CHAPTER 5 CONCLUSIONS

This dissertation proposes two new cascaded multilevel inverter topologies for integrating and managing large scale battery energy storage systems. The control of switching devices in both inverters is done by using a phase-shifted pulse width modulation scheme.

The first proposed isolated multilevel inverter, called Six-Switch Cascaded Transformer (SSCT) multilevel inverter, consists of three phase six-switch converters with ability to reduce number of power components compared with the traditional isolated cascaded H-bridge multilevel inverter. The proposed isolated inverter can be used for high voltage and high power applications such as grid-connected battery storage and alternative energy systems. Using three-phase converters as building blocks enables *dq* frame based simple control and eliminates the issues of single-phase pulsating power, which can cause detrimental impacts on certain dc sources. Simulation studies have been carried out to compare the proposed isolated multi-level inverter with the H-bridge cascaded transformer inverter. The simulation results verified the performance of the SSCT inverter. Although the proposed compact isolated topology does not show advantage in reducing the total amount of harmonics, but the lower order of harmonics in the proposed compact structure inverter have been significantly reduced, which makes it easier to filter out high order harmonics.

The second proposed topology is a Hierarchal Cascaded Multilevel Converter (HCMC) with SOC balancing capability in each phase, which can also be used for high voltage and high power battery systems. The HCMC has a hybrid structure of half-bridge converters and H-bridge inverters and the voltage can be hierarchically cascaded to reach a

desired value at the half-bridge and the H-bridge levels. A phase-shifted PWM modulation scheme has been developed for the proposed converter to guarantee the even utilization of battery modules and the modular design of the converter. Therefore, there is no need of carrier signal rotating strategy, which simplifies the drive circuits and further reduces the cost. Uniform SOC battery management is achieved by controlling the half-bridge converters that are connected to individual battery modules/cells. Moreover, heterogeneous battery modules can be connected in series via H-bridge converters. Simulation studies and experimental results have been carried under different operating conditions to verify the effectiveness of the proposed method.

The results show that individual battery modules can be managed independently on charge/discharge power and bypass control while the overall performance requirement is also met. The THD analysis of the simulation results shows that the THD is increased when there is a bypassed battery module, but not significantly for the affected phases. The three-phase 33-level inverter prototype is implemented based on a digital signal processing (DSP) TMS320F28335 control board. The dc input sources are lithium-ion battery modules with 11.1V rating voltage and 2.2Ah (24.42Wh) capacity. Number of ePWM in the DSP board is limited. So, some other digital control boards such as CPLD and FPGA are needed, which increases design cost. In this work, this limit is addressed by the main program. The control strategy of uniform SOC is based on the open-circuit voltage method. The open circuit voltages can be uniformed by applying the proposed PWM scheme where the measurements are taken every four mints. Battery modules with higher terminal voltages are discharged more. Thus, the SOC equalization or the SOC variation elimination is achieved.

Moreover, a new three-phase SOC equalizing circuit, called six-switch balancing circuit (SSBC), has been proposed for the proposed HCMC or any cascaded multilevel inverters to achieve phase-to-phase SOC balancing to realize uniform SOC operation for the whole battery system. The SSBC can help achieve full utilization of the battery capacity while keeping balanced three-phase operations. A sinusoidal PWM modulation technique is used to control power transferring between phases. Simulation results have been carried out to verify the performance of the proposed SSBC circuit of uniform three-phase SOC balancing.

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ABSTRACT

CASCADED CONVERTERS FOR INTEGRATION AND MANAGEMENT OF GRID-LEVEL ENERGY STORAGE SYSTEMS

by

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This research work proposes two cascaded multilevel inverter structures for BESS. The gating and switching control of switching devices in both inverter topologies are done by using a phase-shifted PWM scheme. The first proposed isolated multilevel inverter is made up of three-phase six-switch inverter blocks with a reduced number of power components compared with traditional isolated CHB. The suggested isolated converter has only one battery string for three-phase system that can be used for high voltage and high power applications such as grid connected BESS and alternative energy systems. The isolated inverter enables *dq* frame based simple control and eliminates the issues of single-phase pulsating power, which can cause detrimental impacts on certain dc sources. Simulation studies have been carried out to compare the proposed isolated multi-level inverter with an H-bridge cascaded transformer inverter. The simulation results verified the performance of the isolated inverter. The second proposed topology is a Hierarchal Cascaded Multilevel Converter (HCMC) with phase to phase SOC balancing capability which also for high voltage and high power battery energy storage systems. The HCMC has a hybrid

structure of half-bridge converters and H-bridge inverters and the voltage can be hierarchically cascaded to reach the desired value at the half-bridge and the H-bridge levels. The uniform SOC battery management is achieved by controlling the half-bridge converters that are connected to individual battery modules/cells. Simulation studies and experimental results have been carried on a large scale battery system under different operating conditions to verify the effectiveness of the proposed methodology. Moreover, this dissertation presents a new three-phase SOC equalizing circuit, called six-switch balancing circuit (SSBC), which can be used to realize uniform SOC operation for full utilization of the battery capacity in proposed HCMC or any CMI inverter while keeping balanced three-phase operation. A sinusoidal PWM modulation technique is used to control power transferring between phases. Simulation results have been carried out to verify the performance of the proposed SSBC circuit of uniform three-phase SOC balancing.

AUTOBIOGRAPHICAL STATEMENT

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