DIGITALCOMMONS
— @WAYNESTATE —

Wayne State University

Wayne State University Dissertations

1-1-2017

Quantum Capacitance Study Of Novel Two- And One-Dimensional Systems

Zhe Wu
Wayne State University,

Follow this and additional works at: https://digitalcommons.wayne.edu/oa_dissertations

Part of the Physics Commons

Recommended Citation
Wu, Zhe, "Quantum Capacitance Study Of Novel Two- And One-Dimensional Systems" (2017). *Wayne State University Dissertations*. 1756.
https://digitalcommons.wayne.edu/oa_dissertations/1756

This Open Access Dissertation is brought to you for free and open access by DigitalCommons@WayneState. It has been accepted for inclusion in Wayne State University Dissertations by an authorized administrator of DigitalCommons@WayneState.

QUANTUM CAPACITANCE STUDY OF NOVEL TWO- AND ONE-DIMENSIONAL SYSTEMS

by

ZHE WU

DISSERTATION

Submitted to the Graduate School

of Wayne State University,

Detroit, Michigan

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

2017

MAJOR: Physics

Approved By:

____
Advisor

____

____

____

© COPYRIGHT BY

ZHE WU

2017

All Rights Reserved

DEDICATION

I dedicate my dissertation work to my family and friends.

ACKNOWLEDGEMENTS

I would like to thank to everyone from quantum transport group. Among them, I want to thank my advisor, Dr. Jian Huang most. Under his guidance, I would be possible to finish my PhD in last five years and write his dissertation. Thanks to other lab mates, Talbot, Vinicio, Parisa. Thanks to Dr. Zhixian Zhou for helping with fabricating devices and suggestion on academia as well as career. Also thanks to my friend Hsun-Jen Chuang and other friends from Dr. Zhou's lab helping with transfer layer structure material. Thanks to Dr. Boris Nadgorny's suggestion in my prospectus and his class in thermal dynamics as well as condensed matter physics. Thanks to Dr. Ratna Naik's encouraging in my PhD. I also want thanks to Dr. Jogindra Wadehra's help with graduate fairs and his electrodynamics class. Thanks to Dr. Ivan Avrutsky for his suggestion on my PhD prospectus. Thanks to Ehab with helping us to use PPMS and discussion. The front desk staffs Deloris Cowen and other people are very nice and helpful. Thanks to my Chinese friend Jinjin Pan, Xinxin Woodward, Xinqiang Cai, Wenquan Zhou, Yu Gao and Shanshan Cao from physics department.

I want to acknowledge NSF funding DMR-1410302 for support.

TABLE OF CONTENTS

Dedication ii

Acknowledgments iii

Chapter 1 Introduction 1

Back ground & Motivation 1

Theory 4

VO_2 introduction 10

GaAs introduction 14

Chapter 2 Fabrication 17

Basic of fabrication 17

Fabrication on GaAs device 18

Fabrication on VO_2 device 29

Chapter 3 Measurement techniques 35

Transport measurement 35

Low temperature 40

Quantum Capacitance measurement 46

Gating and dielectric 52

Chapter 4 Study on Polycrystalline VO_2 55

Polycrystalline VO_2 characteristics 56

Challenges 56

Measurement Method 58

Results 60

Chapter 5 Study on Single crystal VO_2 nanobeam 66
Background 66
Single Crystal VO_2 Characteristics 67
Strain effect 71
Light effect 72
Capacitance on VO_2 single crystal nanobeam 73
Chapter 6 Study on GaAs HIGFET 78
Challenging 78
Results 80
Chapter 7 Other measurement results 85
p-GaAs 85
Graphene result 89
Chapter 8 Summary and future plan 92
Summary 92
Future plan 92
Bibliography 94
Abstract 100
Autobiographical Statement 102

LIST OF FIGURES

Figure 1.1 Diagram for Hubbard model 7

Figure 1.2 Anderson localization picture: Constructive interference of back scattering. 8

Figure 1.3 Two dimensional Wigner crystal[1] 9

Figure 1.4 VO_2 band diagram 12

Figure 1.5 VO_2 Crystal structure: Left: Monoclinic insulating phase; right: Rutile metallic phase 13

Figure 1.6 Quantum well formation: two bulk material in contact. Equilibrium of Fermi level bend the conduction band 15

Figure 1.7 a) GaAsAlGaAs interface TEM pictures. b)Mobility improvement of GaAs.[2] 16

Figure 2.1 a) Shadow mask for sample thin film deposition. b) Shadow mask for metal contacts deposition. c) Finished sample with contacts on it. 18

Figure 2.2 Clean room environment 19

Figure 2.3 Example of GaAs layered structure. Next to the layer material shows the thickness of each layer. The 30X and 70X stands for the replicate times. 19

Figure 2.4 Spin coat substrate with photo resistor 21

Figure 2.5 Karl Suss MJB3 MASK ALIGNER 22

Figure 2.6 Etching rate at different conditions (Room temperature at $69.2°F$, humidity at 47%) 23

Figure 2.7 Etching profile observed by using SEM 24

Figure 2.8 Kurt Lesker Nano36 deposition system platform 25

Figure 2.9 Undercut walls(right) vs no undercut wall(left), The black color is substrate, the blue color is photoresistor 26

Figure 2.10 Major photo lighography procedures 26

Figure 2.11 Anti-Hall bar sample fabrication 27

Figure 2.12 GaAs HIGFET sample fabrication 28

Figure 2.13 Gated p-GaAs sample fabrication 29

Figure 2.14 Schematic of Pulsed laser deposition of Polycrystalline VO_2 31

Figure 2.15 VO_2 single crystal nanobeam synthesis diagram 32

Figure 2.16 Embedded VO_2 nanobeam vs Strain free VO_2 nanobeam 33

Figure 2.17 VO_2 capacitance sample: a) Thin film VO_2 on Si substrate, the p-doped substrate serves as bottom gate. b) Single crystal VO_2 with top gate and bottom gate. 33

Figure 3.1 (a) Schottky barrier forms between metal insulator junction with a height of Φ_B. (b) Ohmic contact I-V curve(orange) vs non-Ohmic contact I-V curve(blue). 35

Figure 3.2 Four terminal measurement setup 37

Figure 3.3 Lock-in amplifier 38

Figure 3.4 Left:Landau levels and fermi energy in a quantum hall system. Right, the longitudinal resistivity and Hall resistivity as function of magnetic field in integer quantum hall effect 38

Figure 3.5 Quantum Hall measurement schematic 40

Figure 3.6 Fractional Quantum Hall effect.[3] 41

Figure 3.7 Structure of inset of dilution refrigerator with different cooling stage . 42

Figure 3.8 a) Currently used sample holder. b) Helium-3 cell sample holder for better cooling purpose. c) Helium-3 cell fillempty control system 43

Figure 3.9 Flow cryostat 45

Figure 3.10 PPMS system 46

Figure 3.11 Schematic for capacitance bridge. 49

Figure 3.12 Ratio transformer bridge measurement circuit. 49

Figure 3.13 Active bridge circuit schematic. 51

Figure 3.14 Circuit for active bridge. (a) Circuit diagram. (b) The picture of real component of the dotted circled area in (a). 53

Figure 3.15 VO_2 gating scenario: (a) gating thin film,(b) gating nanobeam 53

Figure 4.1 Schematic diagram of the free energy as a function of phase parameter.[4] 55

Figure 4.2 Diagram of the polycrystalline VO_2 capacitance device[4]. 56

Figure 4.3 (a) Bridge setup (b) Impedance component in the circuit.[4] 57

Figure 4.4 Comparison of standard in-plane 2-terminal technique (green line) with bridge technique (scatter plots) for measuring sheet resistance. Arrows distinguish between heating and cooling cycles. The in-plane measurement is shown on a semi-log plot in the inset.[4] 61

Figure 4.5 Confirms linear relationship $\mathrm{Im}[V_b] \propto f$ from Eqn. 4.1.[4] 62

Figure 4.6 (a),(b) $\mathrm{Re}[V_b]$ and $\mathrm{Im}[V_b]$ as functions of T. Note the change in scale from μV to mV. (c) $\mathrm{Re}[V_b]$ as a function of $\mathrm{Im}[V_b]$ is a monotonic nearly single-valued function for high frequencies. Inset highlights low frequency measurement where mixing is eliminated. (d) Capacitance changes $\mathrm{d}C_s$ as a function of T. The slope of all traces in the metallic regime gives the T dependence of C_{geo} which has been extrapolated below the MIT as a dashed line.[4] 63

Figure 4.7 (a), (b), and (c) C_s, C_q^{-1} and C_q as functions of T. In (c), only a portion of the thermal cycle is shown, since larger C_q cannot be resolved. [4] . . . 64

Figure 5.1 Left:Resistivity measurement on strained VO_2 on substrate; Right: Resistivity measurement on strain free VO_2 67

Figure 5.2 Growth direction of Single Crystal VO_2 69

Figure 5.3 a), b)Optical image of single crystal VO_2 near transition temperature shows different color alternating strips.[5] c) Schematics of insulating metallic alternating stripes. 70

Figure 5.4 The green arrow indicating the direction of external force applied by tungsten needle. The orange color is the insulating domain.[6] 71

Figure 5.5 UV light effects on VO_2 transition. Left figure shows the strained VO_2 single crystal nanobeam have transition with and without UV light[7]. Right figure shows the similar condition as left when the strain is released 73

Figure 5.6 (a) Optical image of single crystal VO_2 capacitor device. The dielectric is multi-layer hBN, the VO_2 nanobeam and top gate form an capacitor. The thickness of hBN is around 30nm. The length of VO_2 nanobeam underneath hBN is about 20μm. (b) Schematic of side view of the same device. 75

Figure 5.7 (a) Sample capacitance(black line) and fitted geometric capacitance(red line) as a function of temperature.(b) Quantum capacitance C_q. 76

Figure 5.8 (a) Optical image of single crystal VO_2 capacitor bottom gate device. This is an unfinished device, another layer of deposition need to be done on the contacts area. (b) Schematic of side view of the same device. 77

Figure 6.1 (a) The profile after etching, (b) Metal contacts deposition, (c) After annealing, metal contacts have a good Ohmic contacts with 2D layer and have a safe distance from top gate, (d) After annealing, contacts metal are too close to top gate. 79

Figure 6.2 The optical image of a working HIGFET device 80

Figure 6.3 HIGFET turn on test. The inside is a schematic of testing circuit. . . 81

Figure 6.4 Quantum hall measurement on HIGFET 83

Figure 6.5 Temperature dependence on HIGFET 84

Figure 7.1 Shubnikov-de Haas (SdH) oscillations of p-doped GaAs sample[8] . . . 85

Figure 7.2 SdH vs 1/B. 86

Figure 7.3 Dingle factor. 88

Figure 7.4 Effective mass fitted at different magnetic field strength[8], sample B is a similar sample with density p=4.9×10^{10}cm^{-2}, Inset shows our result compared to previous data obtained through cyclotron resonance measurements [9] 89

Figure 7.5 (a)-(i) Differential resistance with variours filling factors, (j) Experimental setup for measuring the bulk conduction properties with separated edges (k) I-V curve from DC measurement at $\nu = 1$ 90

Figure 7.6 a) Quantum hall measurement on ρ_{xx}. b) Dirac point at 77.7K and 292K. 91

CHAPTER 1 Introduction

1.1 Back ground & Motivation

Strongly correlated systems is a fascinating topic in condensed matter physics. Among them, vanadium dioxide(VO_2) is a strongly correlated material which shows metal-insulator transition(MIT) near room temperature(340K)[10]. Early studies have revealed its first order transition nature[10, 11]. Electric transport behaviors as well as optical properties undergoes a tremendous change in the transition[12–14]. These makes VO_2 attractive as a potential functional material in optical switch and semiconductor applications[15, 16]. On the other hand, the transition mechanism of VO_2 is a puzzle for decades. In comparison to traditional correlated Mott insulators, VO_2 also undergoes a huge structural phase transition(SPT) from rutile to monoclinic phases at 340K[10]. Numerous studies have shown strong evidences to support both mechanisms. Structure transition mechanism is supported by optical evidences [17–20]. As for interaction driven mechanism, tungsten doping effects[21] and extreme pressure experiment[22] successfully changes the interaction strength to tune the transition. Nowadays researchers tend to believe both mechanisms contribute to the transition[23, 24]. They occur at identical temperature which hinders researcher to distinguish them. Recent advances have been made thanks to the synthesis of single crystal VO_2 by Guiton's group[5]. With a cleaner and simpler system to study, Ruan's group has implanted optical color depth and TEM diffraction to observe MIT and SPT accordingly. Two transitions can be well distinguished with placing single crystal VO_2 on certain types of substrates [25].

Among research works have been done to study transition mechanisms, few have been done using transport measurements. Even though transport is ideal to study the electronic structure with rich physics, a thorough search of the relevant literature yielded the following:

only two related article measuring hall effect on VO_2[26, 27]; limited number of studies used carrier density tuning method (field effect) on VO_2 also encounter extremely difficult[28, 29] and it remains an open question whether it is due to strongly correlated interaction or short screening length limits the penetration of field effect[30].

To gain a better understanding of the MIT in VO_2 and obtain the electronic structure during the transition, we focus on utilizing quantum capacitance measurement to study VO_2. Quantum capacitance measurement was firstly proposed for probing the electronic structure[31] and have successfully revealed strong interaction in GaAs two-dimensional electron system[32]. Our work has demonstrated a unique method to extract quantum capacitance from a large resistive sample using a home made bridge. The accurately measured capacitance yields density of states(DOS) near Fermi energy which manifests a rapid growth when temperature raises up, as expected for approaching metallic state. Our work is the first experimental study to probe during MIT in VO_2 and is important for unraveling the long-standing mystery behind the driving mechanism for this phase change. Additionally, the bridge method for measuring the quantum capacitance in a highly resistive sample can be readily applied to other systems that exhibit a MIT, which is universal to many systems.

The electron-electron interactions are universal in many systems. Besides Mott insulator which is due to the competition between on-site Coulomb repulsion and transfer integral, 2D charge carriers in confined quantum well also demonstrate behaviors due to e-e interactions. These are fascinating phenomena, but not yet well understood [33–36]. Researchers seek to understand the role of *e*-*e* interactions in ground state. One major question is can *e*-*e* interactions be strong enough to drive 2D charge carriers into lattice structure such as Wigner crystal [37] or Wigner glass [38–40]. For such systems, the Coulomb energy E_C com-

petes with many other factors, such as the kinetic energy E_F, disorder potential, polarizing magnetic field, etc. One of the major challenges to experimental progress in this area, is the difficulty in fabricating high purity systems with dilute charges. Furthermore, making Ohmic contact to dilute charge systems represents a significant challenge. A significant portion of this work is to fabricate ultra-high purity devices using both doped p-type GaAs/AlGaAs quantum square wells and un-doped (capacitively induced holes) heterojunction gated field effect transistors (HIGFETS). These samples demonstrate excellent mobility at low charge densities [41]. These systems allow us to identify pinning behavior in the reentrant insulating phase near filling factor $\nu = 1/3$ in the fractional quantum Hall regime and several signatures of WC without suffering from localization effects [42]. Additionally, these samples provide a unique opportunity to probe the transport between two edges of a topological insulator that are perfectly separated by a bulk insulating phase in a corbino-disk-like geometry for integer filling factors in the quantum Hall regime[43]. These studies are critical to understanding the physics of strongly correlated charges and their relation to topological phases, which is a fascinating area of intense current research [44–48].

The content structure of this thesis as follows: Chapter 1 introduces the physics of strongly interacting systems discussed in this thesis. Chapter 2 presents the fabrication method. Chapter 3 contains the cryogeneic techniques as well as measurement methods we implement. Chapter 4 introduces VO_2 and discusses the quantum capacitance measurement results on polycrystalline VO_2. In Chapter 5 we use single crystalline VO_2 to study the transition. Chapter 6 and 7 represents the result we have from GaAs correlated systems and graphene.

1.2 Theory

1.2.1 Electron in solid, Non-interacting electrons

The behavior of electrons inside solid has been studied for decades. Numerous models have been created for different systems. People started with simple free electron model: For free electrons in metal, in Schrodinger equation, there is no potential energy term. The density of state for 3D can be written as:

$$g(E)\mathrm{dE} = \frac{V}{2\pi^2\hbar^3}(2m)^{\frac{3}{2}}E^{\ \frac{1}{2}}\mathrm{dE} \tag{1.1}$$

Similarly, we can get 2D and 1D density of state. Integrating density of state up to Fermi energyE_F yields the total number of electrons(N), which gives us a formula of Fermi energy as a function of N:

$$E_F = \frac{\hbar^2}{2m}\left(\frac{3\pi^2 N}{V}\right)^{\frac{2}{3}} \tag{1.2}$$

Considering the transport behavior, Drude applied kinetic theory of gases to electrons in metal. It can be described as: $j = \sigma E$ and $\sigma = \dfrac{ne^2\tau}{m_e} = ne\mu_e$

The above model gives a good approximation and it's been widely used. To extend this model to include ions in solid, Born-Oppenheimer approximation is made to decouple electron and ion. The ion and electron has a large mass ratio(2000∼500000) which makes ion relatively static to electron. Another approximation is mean field approximation, which lets one electron treat the interaction from other electrons through an average field. With these approximations, band theory takes the ion potential into account.

The effect of periodic lattice potential on dynamics of the conduction electron wave-

packets can be taken into account by using effective mass m_e to substitute the real mass of electron in the equation of motion. The equation of motion for electrons:

$$\hbar\frac{\mathrm{dk}}{\mathrm{dt}} = -eE \tag{1.3}$$

and group velocity can be written as $v = \frac{\mathrm{d}\omega}{\mathrm{dk}} = \frac{1}{\hbar}\frac{\mathrm{dE}}{\mathrm{dk}}$, Combining these together it gives:

$$\frac{\mathrm{dv}}{\mathrm{dt}} = \frac{1}{\hbar}\frac{d}{\mathrm{dt}}\left(\frac{\mathrm{dE}}{\mathrm{dk}}\right) = \frac{1}{\hbar}\frac{d^2E}{\mathrm{dk}^2}\frac{\mathrm{dk}}{\mathrm{dt}} = -\frac{1}{\hbar^2}\frac{d^2E}{\mathrm{dk}^2}eE \tag{1.4}$$

Also using $m_e\frac{dv}{dt} = -eE$, finally we can define effective mass as:

$$m_e = \hbar^2(\frac{d^2E}{dk^2})^{-1} \tag{1.5}$$

The band theory has been successfully used in many cases in solid state physics[49]. It well distinguishes insulator and conductor, and it gives guidance for engineering the properties of materials. However, people discovered in special cases[50] band theory gives the invalid result.

In certain system[51], when provided with large amount of random disorder, it turns out to be an insulator even there is zero band gap. Anderson studied this disorder driven insulating which is called Anderson Localization. The electron is in phase coherent with its time reversal state. This coherent interference traps electron at the disorder site. The phase coherence can be changed by applying magnet field, which breaks the time reversal symmetry.

In disorder free systems, for example single crystal VO_2 and ultra clean GaAs/AlGaAs

herterojunction, localization of carriers happen as well and leads to insulating behavior. This tells us there are other effects we should take into account which is shown in following section.

1.2.2 Strongly correlated system

When dealing with the interaction among electrons, band theory treats electron-electron interaction in mean field approximation: one electron feel an averaged electric field which is from other electrons around. Is this always true? In most cases, when electron-electron interaction is not dominant effect, it will be overwhelmed by other effects(electrons kinetic energy). The mean field approximation works well when dealing with these cases. For some systems, when interaction between electrons becomes comparable to its kinetic energy, we have to take into account the interaction to get a complete picture.

1.2.3 Hubbard model and Mott transition

Hubbard model is widely used to describe the transition from metal to insulator in Mott insulator. It illustrates interacting particles on a lattice. In modern *ab initio* calculations, the local density approximation is improved by introducing a Hubbard U term to include on-site repulsion effect[52] in transition metal.

For electrons inside solid, tight-binding model only includes the hopping term. Hubbard model has been improved by taking strong interactions into account. Although in most cases, it gives qualitative answer. It successfully predicted Mott insulators which is insulating due to the repulsion between in site electrons.

Hubbard model takes an extra term called on-site repulsion in Hamilton. Which is due to the coulomb repulsion between electrons from same atomic orbitals. As shown in Figure. 1.1, in band theory, there is only the kinetic term which decides hopping(or tunneling) be-

havior. However, by introducing on-site repulsion, Hubbard model considers the competition between hopping and on-site repulsion. Although Hubbard model only considered adjunct site hopping integral and Coulomb repulsion, it is the simplest effective model to take the interaction into account.

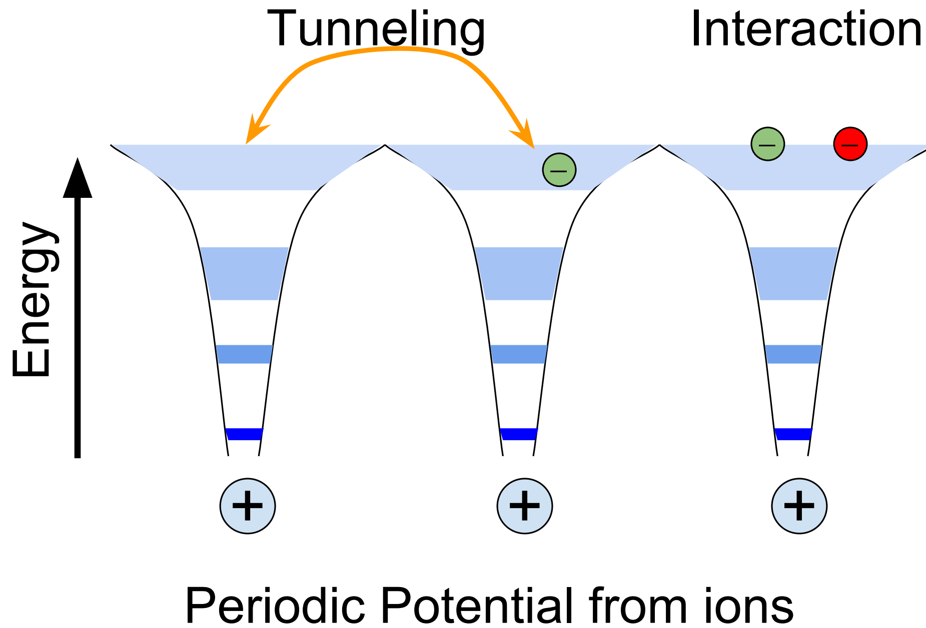

Figure 1.1: Diagram for Hubbard model

The Hamiltonian can be written as:

$$H = H_t + H_U = -\sum_{<i,j>\sigma} t_{ij} c^{\dagger}_{j\sigma} c_{j\sigma} + U \sum_i n_{i\uparrow} n_{i\downarrow} \tag{1.6}$$

The first part H_t is called transfer(hopping) integral, which stands for kinetic energy term. Second part H_U is Coulomb repulsion term called Hubbard U. The typical Mott insulator comes from transition metal oxides, amorphous semiconductors, etc[53, 54]. The system is an insulator when electron-electron Coulomb interaction is larger than its kinetic energy. Why most Mott insulators happens at transition metal oxides? To answer this

question, we have to consider their sub band structure. For transition metal oxides, their 3d band and 2p band has a large gap. When there 3d band is half filled, the H_t is much smaller than those system which has a larger overlapping between out shell band and inner band. In this situation, H_t becomes comparable to H_U term. When H_U is strong enough ,it becomes a correlated insulator. This behavior can be tuned by external gating, carrier injection[10, 55, 56], ultra high pressure as well as doping.

1.2.4 Anderson localization

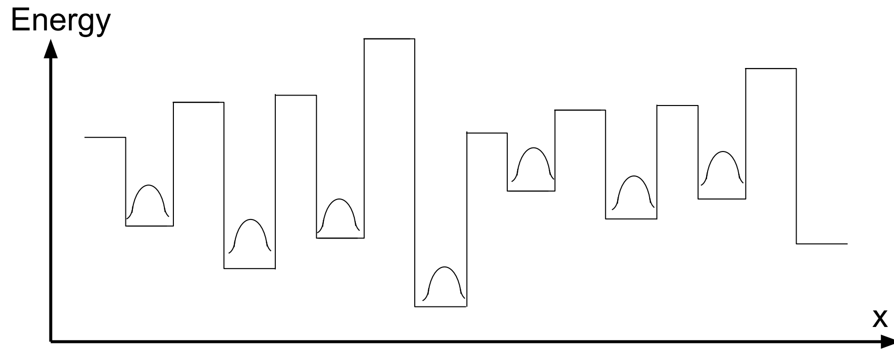

Figure 1.2: Anderson localization picture: Constructive interference of back scattering.

The phenomenon of Anderson localization happens at the ground state. The Anderson localization happens due to the large amount of random disorder. The resistivity temperature dependence of Anderson localization follows Arrhenius hopping. It is predicted as the activated behavior where $\rho \propto \exp{(T_0/T)}$. This provides us with the right way to distinguish the Anderson insulator from Wigner crystal.

1.2.5 Wigner crystallization

Wigner crystal is a solid state phase of electrons. The cause of Wigner crystallization is similar to Mott insulator. Electrons crystallize when Coulomb interaction dominates the kinetic energy. The system indicates insulating behavior. The Wigner crystallization normally

requires ultra low temperature to lower the kinetic energy. For example, the first observation of Wigner crystal is observed on Helium surface where electrons form solid[57]. Compared

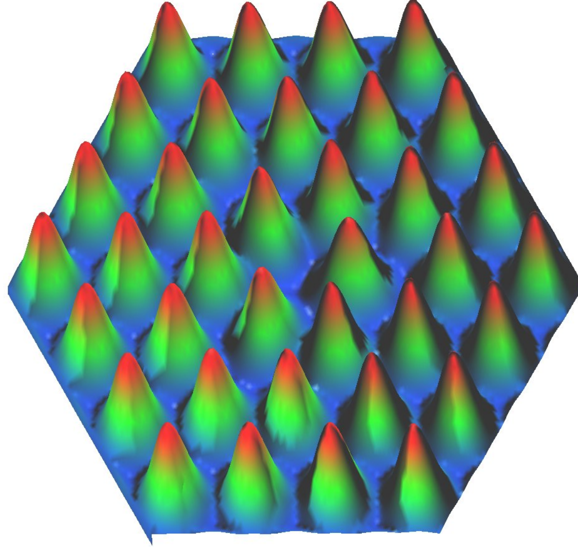

Figure 1.3: Two dimensional Wigner crystal[1]

with Mott insulator which electrons localize at ion lattice site, Wigner crystallization happens when electrons form its own lattice. It happened when electrons are confined within energy potential. As for the Wigner crystal on Helium surface, a potential well formed by the combination of the image potential and repulsive barrier to penetrate into the liquid[57]. The electrons is not moving freely in the 2D surface before Wigner crystallization happens. As an intermediate step, two dimenstional electron gas goes into Fermi liquid before goes to Wigner crystal. With the prove that Wigner crystal exists, naturally the next question is whether Wigner crystal exist inside solid. To achieve Wigner crystal, we need a large r_s value. Several theoretical predictions gives minimum r_s for Wigner crystallization in different systems[58, 59]. All r_s requires to be at least the order of 10. One of the ideal systems people have been found to realize Wigner crystal is quantum well formed in GaAs/AlGaAs

heterojunction. To be able to reach the Wigner crystal, normal it needs to reach a low density to tune up the r_s. From Derude's formula: $\sigma = ne\mu$, when density is too low, there is a trouble to measure electrical signal since the conductivity σ goes down. The only way to resolve this is to achieve a high mobility to compensate the effect from low density. Since GaAs/AlGaAs has a very high mobility, therefore it is an ideal candidate for achieving this goal. Another reason is that GaAs/AlGaAs heterojunction has an almost ideal interface, this fact limits the possibility for the disorder driven Anderson localization. The Wigner crystal are predicted to have a resistivity temperature dependence behivor follows Efros Shklovskii hopping. It is a non-activated behavior where $\rho \propto \exp{(T_0/T)^{1/2}}$. This provides us the very important way to distinguish Wigner crystal from Anderson insulator.

1.3 VO_2 introduction

VO_2 is a strongly correlated material. It attracts attention due to its near room temperature Metal insulator transition(MIT). VO_2 undergoes transition from insulator to metal around 340K[10]. The resistivity during the transition changes many orders. There are only few materials has MIT transition near room temperature: VO_2(340K), NbO_2(1080K), Ti_2O_3(410K), and V_2O_3(150K)[10, 60]. Among them, VO_2 shows closest transition temperature to room temperature. It also shows first order transition which happens with abrupt properties changes on electrical conductivity, optical transmittance. These features make VO_2 potential for electronic applications including fast switches, sensors, memories.

The electron-electron interaction in VO_2 can not be ignored when study the electrical properties. However, electron-electron interaction is not the only mechanism for transition. The structure of VO_2 changes from monoclinic insulator to rutile metal. The transition happens with hysteresis. Depending on the crystal structure, the hysteresis can be progressive

Phase	Symmetry	Lattice Constant(Å)			Angle
Rutile	$P4_2/mnm(D_{4h}^{14})$	a_R=4.55	b_R=4.55	c_R=2.86	90°,90°,90°
Monoclinic	$P2_1/c,(C_{2h}^5)$	a_{M1}=5.38	b_{M1}=4.54	c_{M1}=5.75	90°,122.6°,90°

Table 1.1: Rutile and Monoclinic phase comparison

for multi-grain sized VO_2[10], or cascade for single crystal VO_2[5]. Although the hysteresis is not favored for application, there is no good method can suppress the hysteresis effectively.

1.3.1 Physical and electronic structure of VO_2

The phase transition is a first order transition. When temperature belows T_c(340K), VO_2 is in monoclinic ($P2_1/c$) phase. The characteristics of this phase is the V^{4+}-V^{4+} pairs in c axis have alternate separations of 2.63Å and 3.12 Å as shown in left of Figure 1.5. Compared with the rutile metal phase when temperature is higher than T_c, the V^{4+}-V^{4+} pairs has a fixed separation of 2.86Å. The structural difference causes the number of V^{4+} in unit cell doubled from metal phase to insulator phase. However, since the monoclinic phase now has almost as twice length on c axis. This makes the experimental observable change rather smaller. In fact on single crystal VO_2, the experiments[61, 62] work has shown there is about 1% expansion from rutile phase to monoclinic phase.

Table 1.3.1 shows the lattice comparison.

The band gap of VO_2 has been studied by different means, the optical studies shows: the band gap is 0.2∼0.3 eV for rutile metal state; for monoclinic insulating state, optical band gap is 0.6∼0.7 eV[12, 63]. The relationship between MIT and electronic structure of VO_2 are qualitatively explained by Goodenough in 1971[64]. In this work, he proposed the Peierls-type structurally-driven MIT model to explain the MIT behavior. The vanadium atom has electron configuration $[Ar]4s^23d^5$, this atom bound to two oxygen atoms has the

$1s^2 2s^2 2p^4$ configuration. Four electrons of vanadium fill oxygens' shell. The Vanadium atom has a single electron left near its fermi level. The electrons in O atom form a closed shell and lie below the fermi level. Because of the anistropic crystal field. The level where the electrons reside are split into two level manifold(e_g) and three level manifold(t_{2g}). The t_{2g} state again splits into $d_{//}$ and d_π states. The $d_{//}$ and d_π states overlap with $d_{//}$ filled with a single electron on the bottom. Fermi level lies in d band, which makes it rutile metal phase as shown in Figure 1.4. As for the monoclinic phase, the V^{4+}-V^{4+} paring parallel to the c-axis splits the $d_{//}$ band into bonding and antibonding states. An energy gap about 0.6eV∼0.7eV is formed between $3d_{//}$ band and $3d_\pi^*$ band in Figure 1.4 (a).

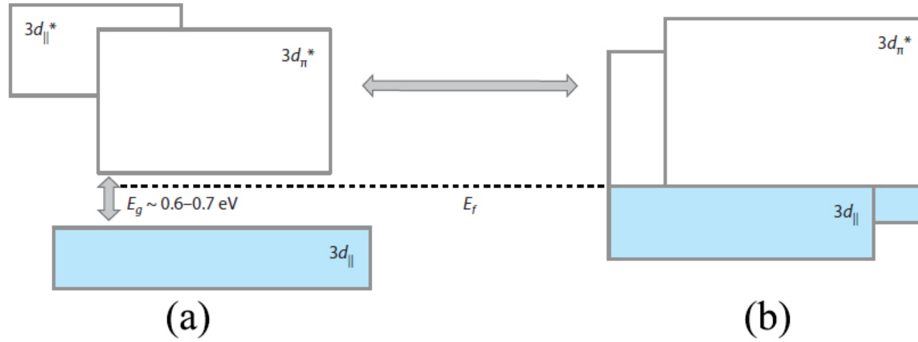

Figure 1.4: VO_2 band diagram

1.3.2 Mott transition vs Peierls transition

The challenging to study VO_2 transition is complicated by the entanglement of Mott transition vs Peierls transition(Structure transition). As discovered by Morin in 1959[10], VO_2 has been the focus of research. However, when VO_2 electronic structure changes with temperature, its structures also changes. Both transition happens about the sample temperature(340K). There has been a long debate about which transition dominate the transport properties as well as optical properties[17, 65–69]. Recently, the synthesis of single crystal

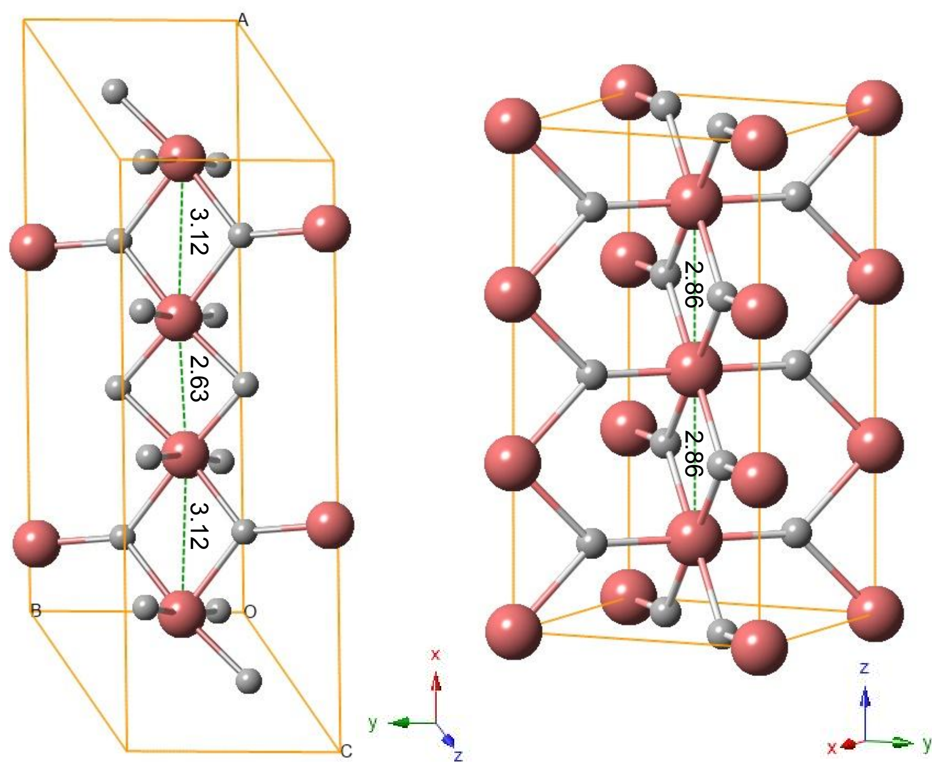

Figure 1.5: VO_2 Crystal structure: Left: Monoclinic insulating phase; right: Rutile metallic phase

VO_2[61] has enabled another approach to study at VO_2 metal insulator transition.

1.4 GaAs introduction

Another strongly correlated system used in this study is GaAs/AlGaAs heterostructures as shown in Figure.1.7 (a). Aluminum gallium arsenide ($Al_xGa_{1-x}As$) is a semiconductor nearly the same lattice constant as GaAs. It has larger bandgap than GaAs. The x in the formula above is a number between 0 and 1. This indicates an arbitrary alloy between GaAs and AlAs. The advantage of GaAs/AlGaAs heterostructures is that the mismatch of the lattice between GaAs and AlAs is very small (AlAs's lattice constant is 0.15% larger than GaAs's) in Figure.1.7 (a). This allows the heterostructures formed in GaAs/AlGaAs to have very little impurity and induced strain. As a result, it has the highest electron mobility in record. The highest mobility record of GaAs/AlGaAs heterostructures is $36,000,000\ \mathrm{cm^2/\,Vs}$ [70]. To make a comparison, the highest mobility in MOSFET is roughly $80,000\ \mathrm{cm^2/\,Vs}$. The device we used in our study is confined electrons in two dimensions. Normally by tuning the dimensions of system, we expected different physical properties. For example, the magnet moments and local volume have different in various dimentions[71]. The single electron device is based on zero dimension electrons[72].

After two type of semiconductors are placed in contact to form the heterostructure, rearrangement of mobile carriers which occur near the compositional junction. As a result, electrons move from the semiconductor with the higher Fermi-level to the other, and an electric field is produced to balance this transfer. At end an equal fermi level is reached. The built in potential tilts the conduction band at the interface to have a local energy minimum, a confined quantum well is formed as illustruted in Figure.1.6. Another type of quantum well can be created by applying sandwich structure($Al_xGa_{1-x}As$-GaAs-$Al_xGa_{1-x}As$).

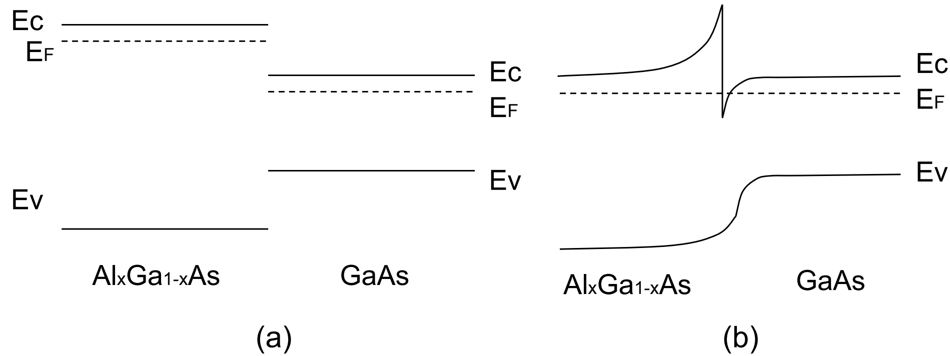

Figure 1.6: Quantum well formation: two bulk material in contact. Equilibrium of Fermi level bend the conduction band

Most GaAs/AlGaAs heterostructure has a delta doping layer next to it. Delta doping supplies charge carriers, usually Carbon for P doping and Silicon for N doping. Delta doping is known to cause much less imperfection than normal doping method. However, this small sacrifice of quality becomes critical in situation to distinguish Anderson localization(disorder caused) or Wigner crystallization(interaction caused). To achieve almost no imperfection is to grow undoped GaAs/AlGaAs heterostructures. For this type of structure, there is no intrinsic dopant. Carriers are only capacitively induced by a metal gate, and the carrier density is controlled by the gate voltage. This is the concept of a HIGFET illustrated in details in Chapter 6.

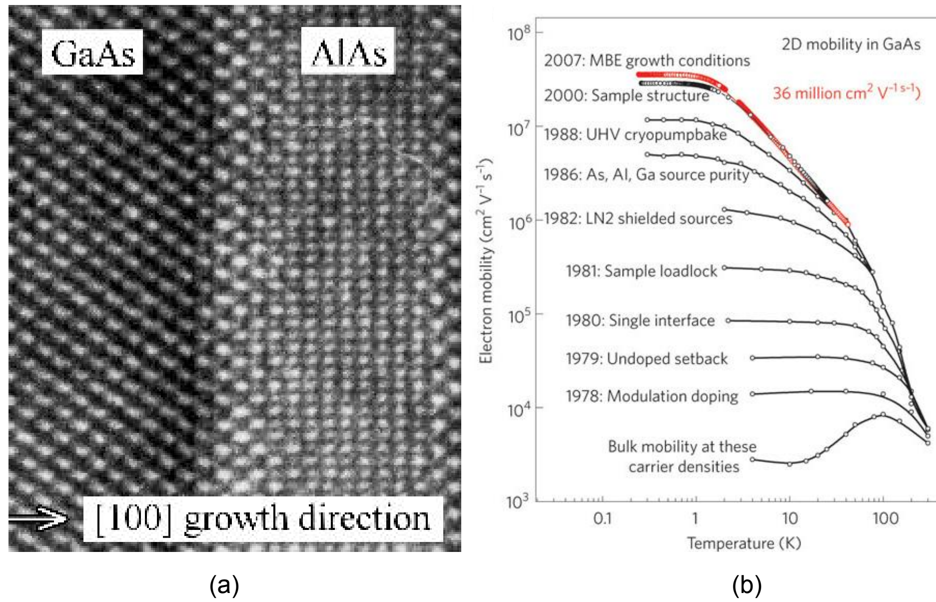

Figure 1.7: a) GaAsAlGaAs interface TEM pictures. b)Mobility improvement of GaAs.[2]

CHAPTER 2 Fabrication

2.1 Basic of fabrication

2.1.1 Shadow method

Shadow masking is a simple technique. The masks we have designed are 1 inch diameter circular stainless steel sheet. The patterns are created by intense laser burning. This method usually has been used in large sample and making contacts to it. This method is usually used in making thin film like sample. The masks are in pair. One mask for growing sample(Figure 2.1 a), the other mask for making contacts(Figure 2.1 b). Mask shown in Figure 2.1 a is used to attach to the substrate wafer, the sample material will be evaporated on to the substrate through the opening on mask. When the growth is done, the substrate has the thin film in the shape shown in Figure 2.1 a. Next step, mask in Figure 2.1 b is used. Three small patterns on the rim serves as the alignment mark. The masks and wafer need to be well aligned to guarantee the location of the contacts on right position. The contacts are made by thermally depositing metals(We use Au/Cr.). The contacts deposition will form the same shape as the pattern in Figure 2.1 b. This method has been used to make VO_2 polycrystalline sample on SiO_2 substrate. Figure 2.1 c shows a finished 1 inch wafer with various patterns on it.

2.1.2 photolithography

Photo-lithography is the first step in nano-fabrication. All the modern computer chips are manufactured by Photo-lithography. In industry, the Extreme Ultraviolet Lithography(EUV) is used to make the fabrication resolution approaching 10nm[73]. At Wayne state university, our lithography equipment(MJB-3) has a resolution of 0.6μm. Most times the resolution we can approach is also limited by the microscope on MJB-3. Consider all these

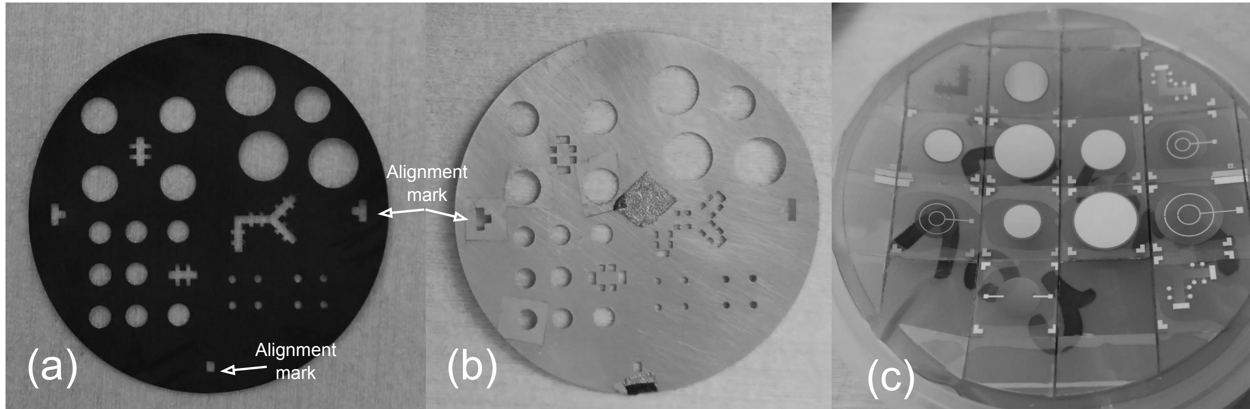

Figure 2.1: a) Shadow mask for sample thin film deposition. b) Shadow mask for metal contacts deposition. c) Finished sample with contacts on it.

factors, we have an estimated accuracy of 2 μm aligning the pattern. Below are several steps for the photo-lithography, the schematic diagram is illustrated in Figure 2.10:

2.1.3 Clean room environment

Our devices are all fabricated in a class 100 cleanroom in physics department at Wayne state university. The temperature and humidity are well controlled in desired range by airtech system. The temperature in our clean room is 68±2°F. The humidity is controlled 48±3%. The condition is crucial for the success of fabrication.

2.2 Fabrication on GaAs device

The GaAs wafer used in our lab are provided by our collaborators from Princeton University and Sandia National Laboratories. The wafers are made with well defined layered structures form GaAs-AlGaAs quantum well(See Figure 2.3). The works we did in Wayne state university include making the raw wafer into different electronic device for various measuring purpose.

The fabrication includes the following major steps:Lithography, Etching, Metal deposition, Making Ohmic contacts. Following illustrates these steps.

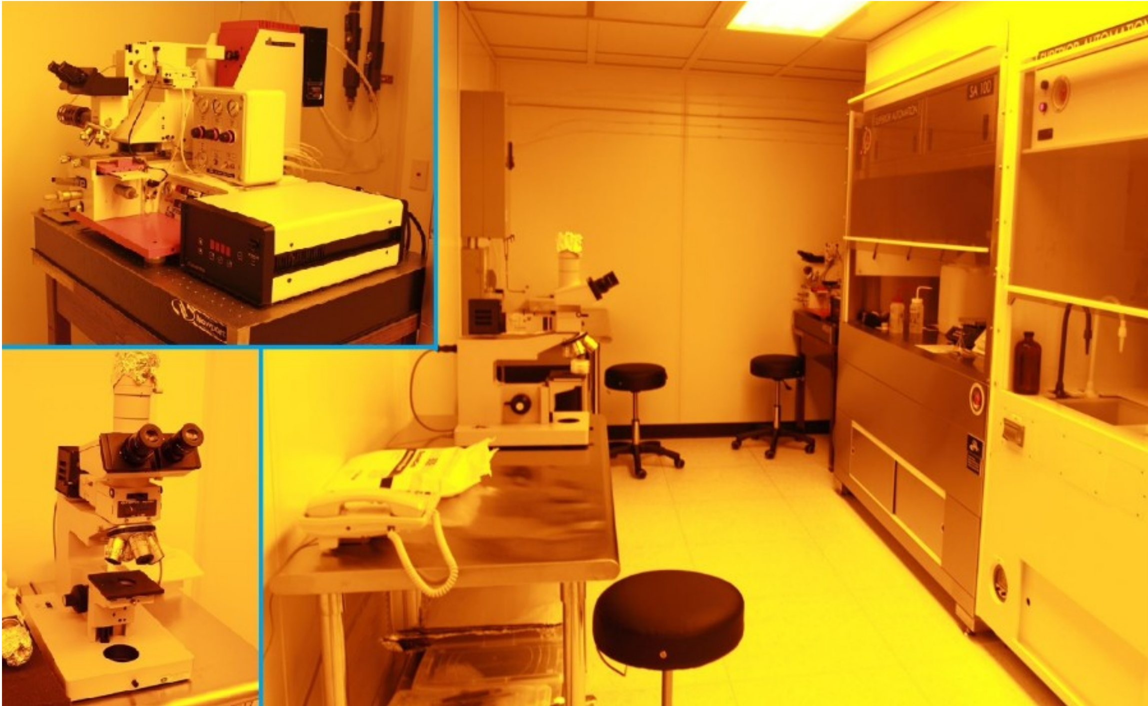

Figure 2.2: Clean room environment

Label	Layer	Thickness	Repeat
	GaAs	70 Å	
δ doping →	$Al_{0.3}Ga_{0.7}As$	60 Å	
2DEG →	$Al_{0.3}Ga_{0.7}As$	500 Å	
	GaAs	2000 Å	
	GaAs	200 Å	30X
	$Al_{0.3}Ga_{0.7}As$	210 Å	30X
	GaAs	2500 Å	
	GaAs	100 Å	70X
	$Al_{0.25}Ga_{0.75}As$	100 Å	70X
	GaAs	500 Å	
	GaAs	2000 Å	
	Bulking semi-insulating GaAs(100)		

Figure 2.3: Example of GaAs layered structure. Next to the layer material shows the thickness of each layer. The 30X and 70X stands for the replicate times.

2.2.1 Lithography

The purpose of lithography is to make a thin film (1∼2 μm) material with certain patterns. The opening on the pattern exposes the sample surface. This part of the sample can be etched away and deposit metal to make Ohmic contacts.

Spincoat

Spin coating is a common techniques for applying thin films to substrates. It is widely used in industries and research. It can quickly and easily produce uniform films, the thickness ranging from a few nanometres to a few microns. In our fabrication, firstly, spin coat the sample with photo-resistor. The photo resistor is dropped on sample which form a dome shape in Figrure 2.4 a. Then the substrate is rotated at high speed on spinner and the most of photo resistor fly off the substrate(Figure 2.4 b). For a large wafer spin coating, the air is blowing from top on to the photo resistor. In our lab, we don't apply air flow since the samples we use have a small size($<1\text{cm}^2$). After spin, the photo resistor left on substrate forms an uniformly thin film. The photo resistors we commonly used in our clean room are AZ4620 and Shipley S1811/S1813. Both are negative photoresistor. The spin speed-thickness relation can be found in photoresistor data sheet. A good estimation can be done using $t \propto \frac{1}{\sqrt{\omega}}$. We normal use a thickness larger than 1μm photoresistor.

Soft-bake

After spin-coated, the photoresistor need to be soft-baked before using. Solvents can be removed during Soft Baking. The photoresistor becomes photosensitive only after softbaking. The baking time and temperature varies with photoresistor type. See the Table 2.1 for soft bake details. The soft baking temperature and time need to be well controlled. Over

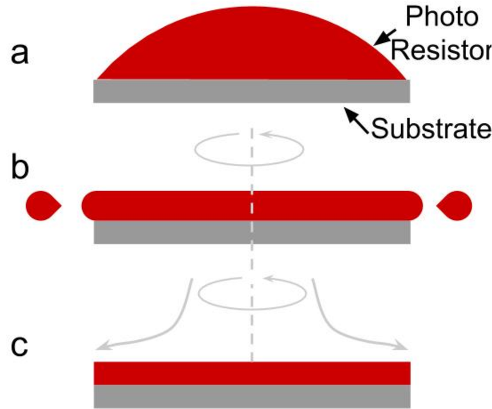

Figure 2.4: Spin coat substrate with photo resistor

baking can degrade the photosensitivity of photoresistor. Under baking can prevent UV light during the exposure procedure. If the sample has been soft-baked but left in a high moisture environment for a long time, it is necessary to soft bake it again.

Photoresistor	bake type	temperature($^{\circ}C$)	time(s)
AZ4620	soft	95	95
AZ4620	hard	105∼110	180∼300
S1811	soft	115	60
S1813	soft	115	60

Table 2.1: Table to test captions and labels

Expose pattern

To expose pattern, we use Karl Suss MJB3 mask Aligner to align the pattern on the mask to the sample. After alignment, a 365nm UV light is uniformly exposed to the sample. The expose time can be derived from formula: $\frac{Dose}{UV intensity}$ The photoresistor specific required dose can be found from the photoreisitor data sheet. The typical exposure time used in our samples is ranging from 15 to 27s.

Development

After exposure, the sample can be developed using developer. The developer used for GaAs is AZ400K diluted with DI H_2O at ratio 1:5. The development time can be found in

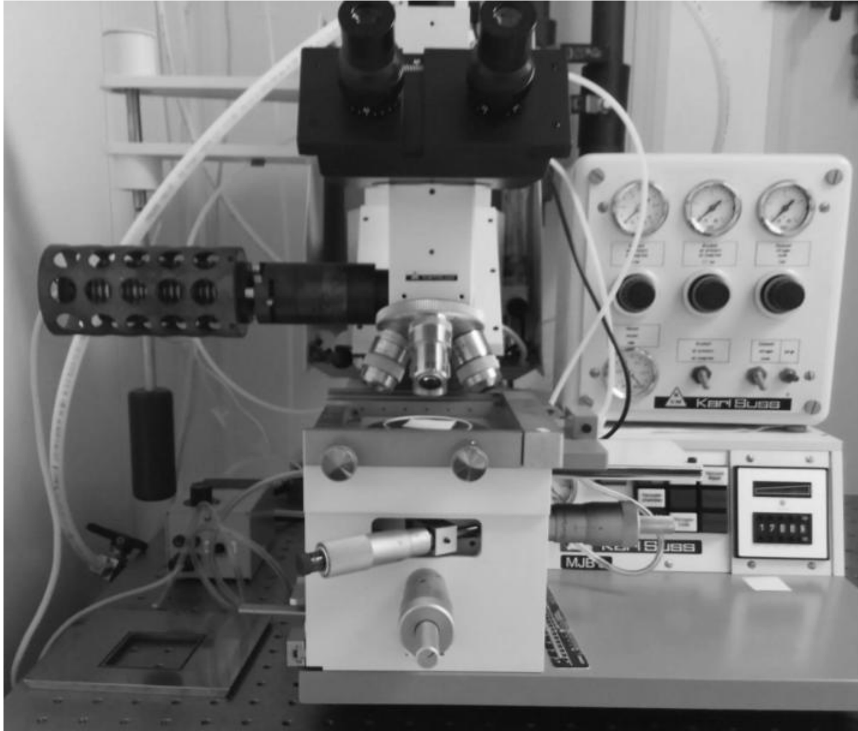

Figure 2.5: Karl Suss MJB3 MASK ALIGNER

photoreisitor data sheet. To develop the photoresistor, the exposed sample is immersed into a baker with developer. To have a rough estimated develop time for large patterns(visible). We develop until exposed pattern become clear and wait for extra 5s before immerse into DI water.

Hard-Bake(post expose bake)

The hard-bake is used to harden the resist image after development. Similar to soft-baking, during this step sample will be put on surface of hotplate. This step will make photoresistor withstand the harsh environments of etching. Usually high temperatures are used (100C - 120C). Such high temperature will crosslink the resin polymer in photoresistor. By doing this, the photoresistor image becomes more thermally stable. Hard-bake also helps to improve photoresistor adhesion to the wafer surface. The only photoresistor we have been used for hard-bake is AZ series. The temperature and baking time is shown in Table 2.1.

Etching

Etching on GaAs devices are all done by using wet etching. The enchant are made of H_2O_2, H_2SO_4, H_2O in a ratio of 4:5:16. Two type of etching condition has been used in this thesis:

Etching in the light: Etching in the light is more generally used define a hall bar pattern on the sample. For p-doped sample, photoresistor protect the hall bar pattern, the rest will be etched away by using etching in the light, leave buffer substrate. For undoped HIGFET sample, the light etching will etch away the area except the gate region.

Etching in the dark: Dark etching is only used for HIGFET contacts etching in this work. As shown in Figure 2.6, the dark etching has a slight low etch rate(8.66 nm/s) than light etching rate(8.99 nm/s). However, the profile of dark etching are different from light etching.

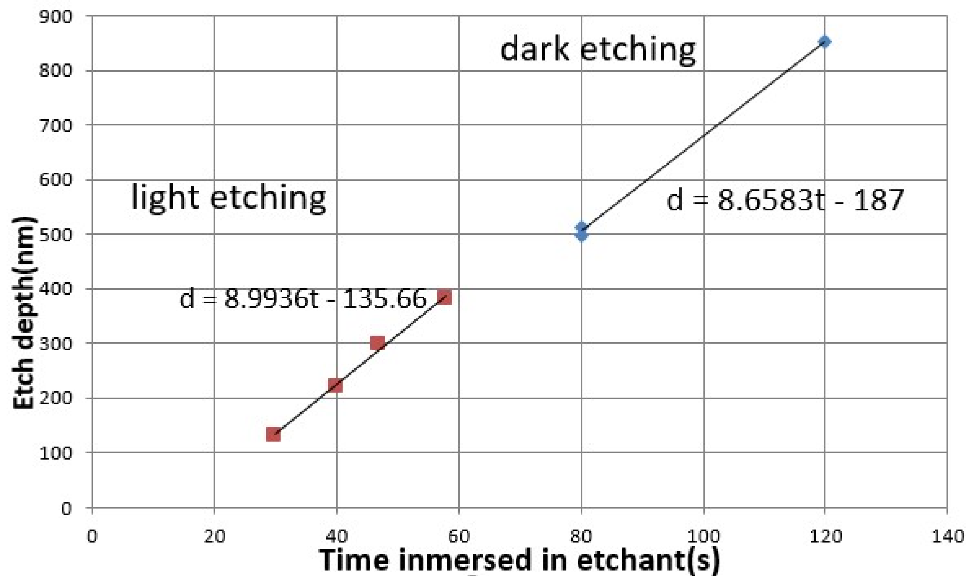

Figure 2.6: Etching rate at different conditions (Room temperature at 69.2°F, humidity at 47%)

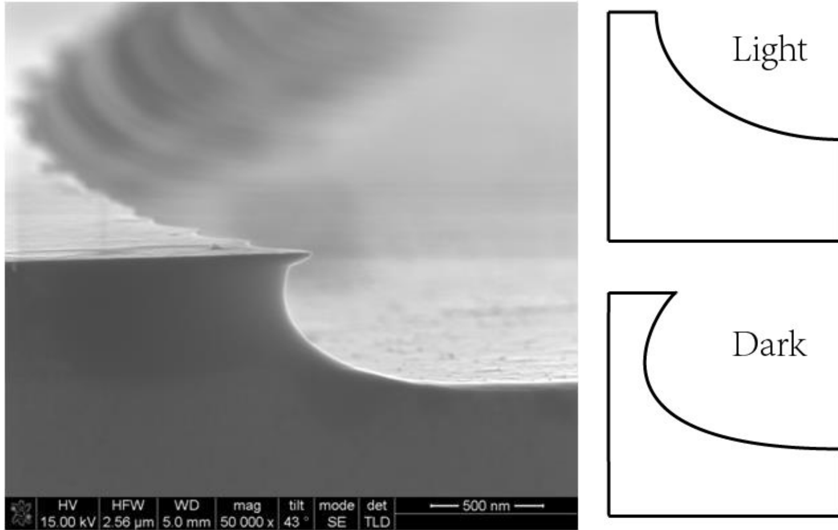

Figure 2.7: Etching profile observed by using SEM

2.2.2 Metal deposition

Thermal evaporation of metal

Deposition of metal can make ohmic contact to the sample. The developed sample has photoresitor patterns. These patterns has opening like windows allow the evaporated metal to go through. Sample is anchored to a round metal plate inside vacuum chamber(Figure 2.8 a). This plate can rotate and tilt to a certain angle. Metal source is heated with a large current to evaporate. During the evaporation, the thickness of deposition is recorded by a film thickness monitor down to $1\AA$. The depositing instrument we used in our lab is nano 36, with powerful turbo pump it can quickly pump down to 3E-8 torr. This level of high vacuum is helpful for making a good deposition. Also, a good vacuum can prevent the metal from oxidization during the evaporation. During each deposition, the chamber pressure of Nano 36 is under 2E-6 torr. There are two type of metal deposition. The contact metal and gate metal deposition. Deposition recipes are listed in Table 2.2.

Liftoff

Liftoff is the last step in lithography. Finally, after the deposition is done, the sample

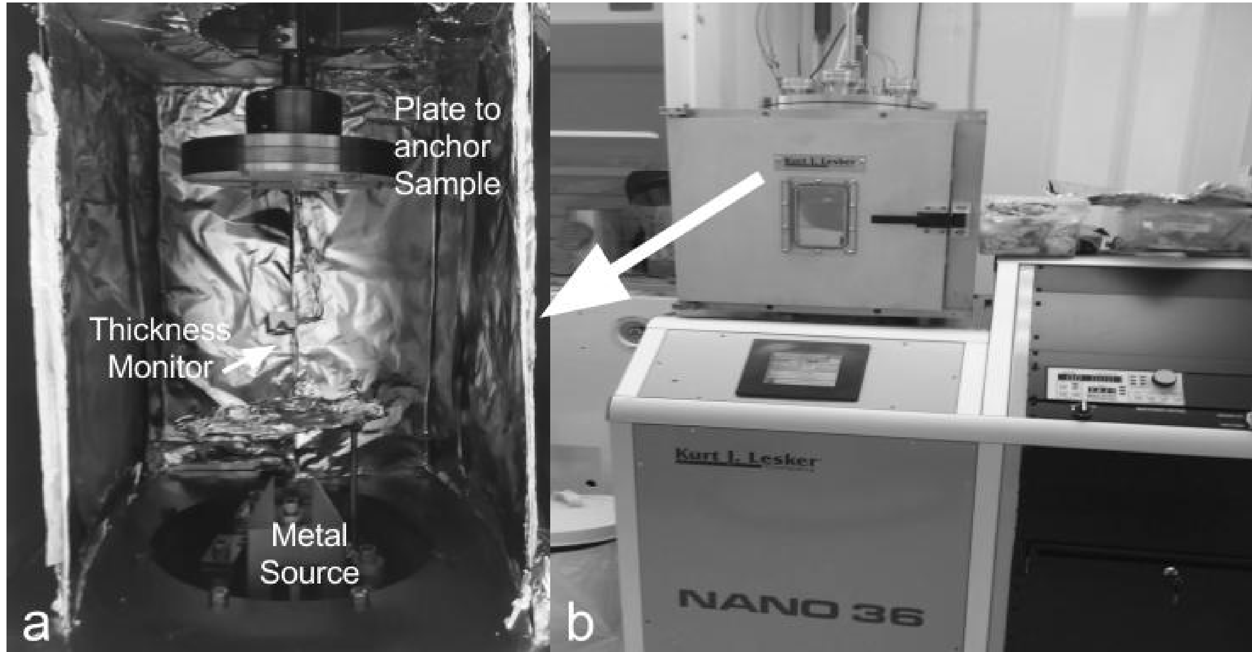

Figure 2.8: Kurt Lesker Nano36 deposition system platform

Device	type	material 1	thickness(nm)	material 2	thickness(nm)
p-GaAs	contact	AuBe	95	Au	5
p-GaAs	gate	Cr	30	Au	15
HIGFET	contact	AuBe	160	Au	10
HIGFET	gate	Cr	30	Au	15
n-GaAs	contact	AuGe	70	Au	5
n-GaAs	gate	Cr	30	Au	15

Table 2.2: Table of metal deposition

will be soaked into acetone to remove the photoresistor. There are a few factors can effect the liftoff, which need to be considered. The first thing is the exposed pattern need a good undercut wall to guarantee the liftoff. The idea of under cut is shown in Figure.2.9. This corresponds to the develop step in Figure.2.10. If the under cut is not good enough, the deposited metal can connect as one whole piece, and acetone wont go though the metal to clean the photoresistor. Secondly, the surface has to be kept as clean as possible. If there are dust or small dots on the surface. They can pin the photoresistor when during liftoff. Lastly, The metal deposition has to be done in a sufficient low pressure, otherwise, the thermal

evaporated metal particles can carbonize the photoresistor.

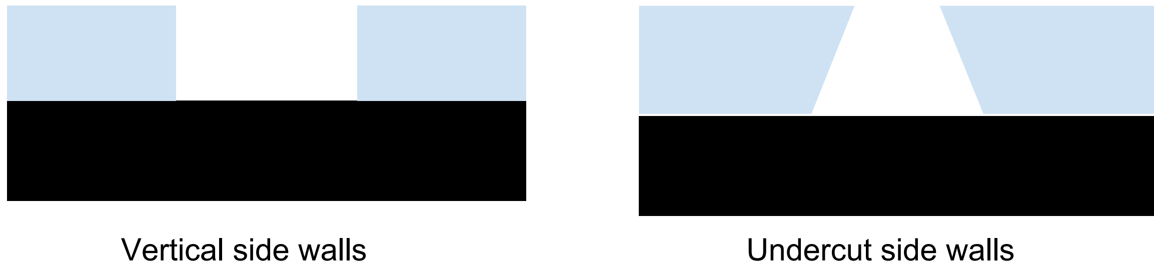

Figure 2.9: Undercut walls(right) vs no undercut wall(left), The black color is substrate, the blue color is photoresistor

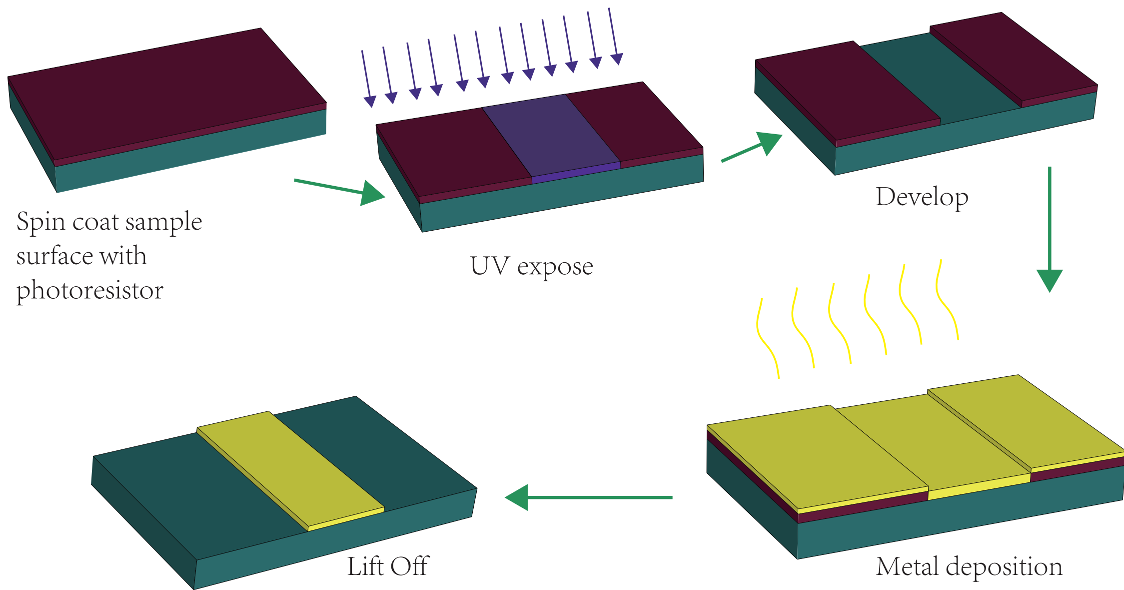

Figure 2.10: Major photo lighography procedures

2.2.3 Making Ohmic contact

The Ohmic contacts are important for a working electronic devices. To make an ohmic contact. After lift off, the device will be put into forming gas and annealed at high temperature to overcome the Schottky barrier.

For p-doped GaAs device sample, annealing has been done at $485°F$ for 10 minutes. The chamber has been preconditioned with flushing forming gas. The forming gas used in our

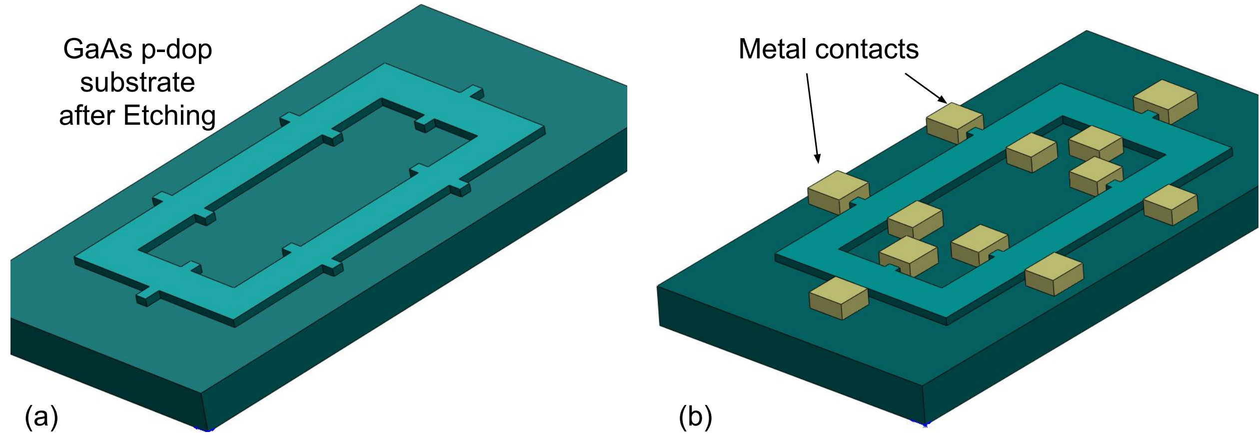

Figure 2.11: Anti-Hall bar sample fabrication

lab is 5%H_2+95%N_2. When sample surface temperature reached 485°F, the forming gas stops flushing and the chamber pressure stays around 350 mbar.

2.2.4 Three types of GaAs sample

Anti hall bar sample

Figure 2.11 shows the anti hall bar sample fabrication. The p-doped GaAs sample is photolighography with light green pattern in Figure 2.11 a. Then elsewhere is etched down below 2D hole layers(About 500 nm for p-type GaAs sample used in this work). After etching, only the square-donut part has a 2D hole layers, elsewhere is left with semi-insulating GaAs bulk substrate layer(Figure 2.3). After this square donut, another lithography need to open 12 windows on the metal contacts area shown in Figure 2.11 b. The mask is used has to be in pair with the first mask. The patterns are self alighed through the alignment mark. Finally the contacts need to be annealed with forming gas at certain temperature to form ohmic contacts.

GaAs HIGFET sample

HIGFET stands for Heterostructure Isolated Gate Field Effect Transistor. In this work, HIGFET is GaAsAlGaAs without doping. Unlike doped GaAs material, HIGFET has no

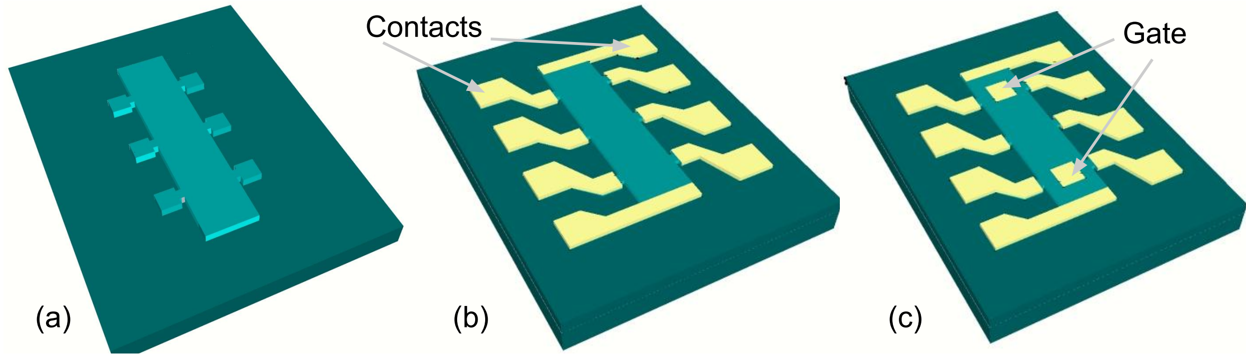

Figure 2.12: GaAs HIGFET sample fabrication

intensional doping, all the carriers comes from field effect. The HIGFET sample has a heavily doped layer on surface which is grown by MBE. This heavily doped layer serves as the top gate. To fabricate HIGFET, we firstly make a standard Hall bar using photolithography. Then the Hall bar area is protected and elsewhere is etched down, the etching depth depends on the sample structure. After etching, the sample is shown in Figure 2.12 a. This step will guarantee only the Hall har area has the 2D interface. The following step is depositing metal contacts and annealing. The metal thickness, annealing time and temperature are tricky parameters which need to be fine tuned to obtain a functioning device. Details about this step is discussed in Chapter 6. After contacts have been made, the final step is depositing metal to the gate. Since the same itself has a heavily doped layer, we only need to deposit metal to the surface. Note this step is not deposting the gate, depositing two square as shown in Figure 2.12 c can prevent surface oxidation as well as making it easier for wiring.

Gated p-type GaAs sample

The gated p-type GaAs sample is a standard hall bar measurement setup with a metal top gate. To fabricate this type of sample, metal contacts are firstly deposited on surface of GaAs. Contacts are annealed at 485°C for 10 minutes to form ohmic contacts. Secondly,

a top metal gate is deposited in the center of the sample. The position of metal gate is controlled by alignment mark. Then, another lithography is used to make a layer of photoresistor to protect the area connecting metal contacts and metal gate. Lastly, etching removes the the uncovered area. Both photoresistor protected and metal protected area will stay. The p-doped GaAs sample we used in our research has no heavily doped surface layer. In another words, the metal gate defines the 2D carrier area. The gate has to be made before etching away the unprotected material so that the 2D carrier is well covered by metal gate. This way reduces the gap or any misalignment between top gate and 2D layer. The contacts have to be produced before top gate, otherwise, annealing contacts will short the top gate to 2D layer.

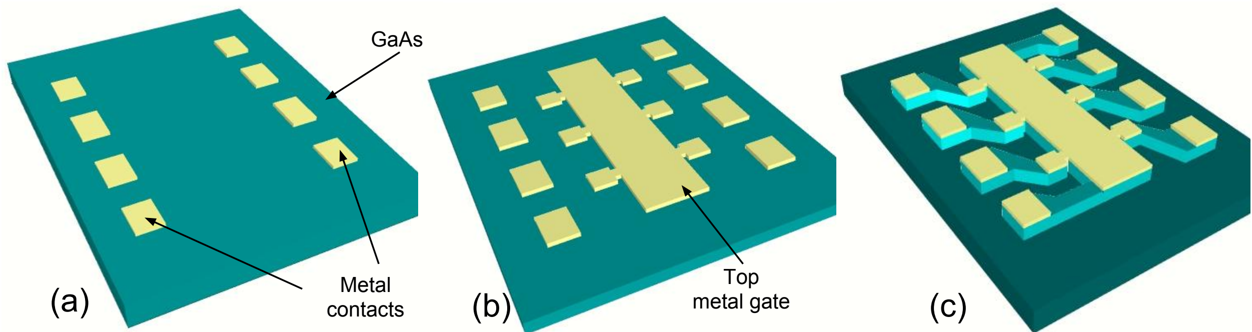

Figure 2.13: Gated p-GaAs sample fabrication

2.3 Fabrication on VO_2 device

There VO_2 devices in this work include VO_2 film based and VO_2 nanobeam based. For VO_2 film, making a device is not difficult. Even without lithography, putting silver paint on VO_2 film yields good contacts. This section focus on the fabrication of VO_2 single crystal nanobeams.

2.3.1 Polycrystalline VO_2 preparation

Vanadium dioxide thin film can be synthesized from metal-organic chemical vapor deposition method[74], physical vapor deposition[75], pulsed laser deposition(PLD), sputtering and sol-gel[76–78].

In this thesis, $VO2_2$thin film was deposited through pulsed laser deposition on the SiO_2 thin layer. Our thin film VO_2 sample is from Dr. Nelson Sepúlveda's group in Michigan State University. As shown in Figure 2.14, the substrate was placed into a vacuum chamber with oxygen gas pressure at 20 mTorr. A metallic vanadium target was ablated using a KrF excimer laser was ablated by excimer laser pulses with energy of 352 mJ per pulse (fluence of ∼2 J/cm2) and a frequency of 10 Hz. A ceramic heater used to heat the sample was maintained at 595 °C through 25 min deposition. Following the deposition, 30 min annealing process was performed with the same deposition conditions[79]. The single crystal nanobeam of VO_2 in this thesis is synthesised by physical vapor deposition[5]. The schematic for physical vapor deposition is Figure 2.15, V_2O_5 powder source is placed in a ceramic boat located in the center of a tube furnace setup, and a silicon substrate with SiO_2 covered surface is placed 3 ∼ 5cm away from the edge of the boat in the downstream direction. Argon flows into the tube at a constant rate as a carrier gas, and a mechanical pump maintains the tube in vacuum. Then, the furnace temperature is ramped to 900 ∼ 950°C in 30 min, and is maintained for 30 min before cooling down naturally. The flow parameter has to be controlled to make single crystal VO_2 nanobeam. The thickness and width of nanobeam are usually from 40 nm to 2 μm. The length can goes up to hundreds microns.

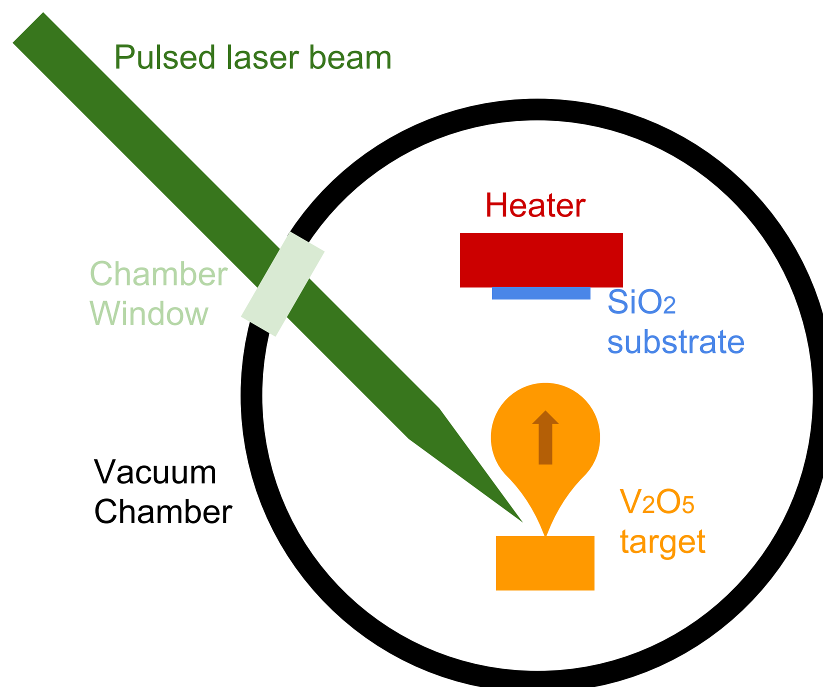

Figure 2.14: Schematic of Pulsed laser deposition of Polycrystalline VO_2

2.3.2 Single crystal VO_2 preparation

Our single crystal VO_2 nano beam is provided by our collaborator from Dr. Jie Yao's research group at the University of California, Berkeley and Jiwei Hou from Tsinghua university at Beijing. Vanadium dioxide single crystal nano beam are grown at a rather high temperature 900-1100°C[5]. Although this temperature is lower than melting point of SiO_2(1600°C), this temperature soften SiO2 substrate and embedded VO_2 into the SiO_2, which results in a large strain along the c-axis. This external strain cause the transition temperature much higher and the transition is not sharp. To reduce this strain effect. Buffered oxide etch(BOE) is used to etch a very thin SiO_2 layer. After the SiO_2 around VO_2 nanobeam is reduced , some VO_2 nanobeams then become loosely bonded to the substrate and therefore can be transferred on to another SiO_2 substrate using micro-manipulator.

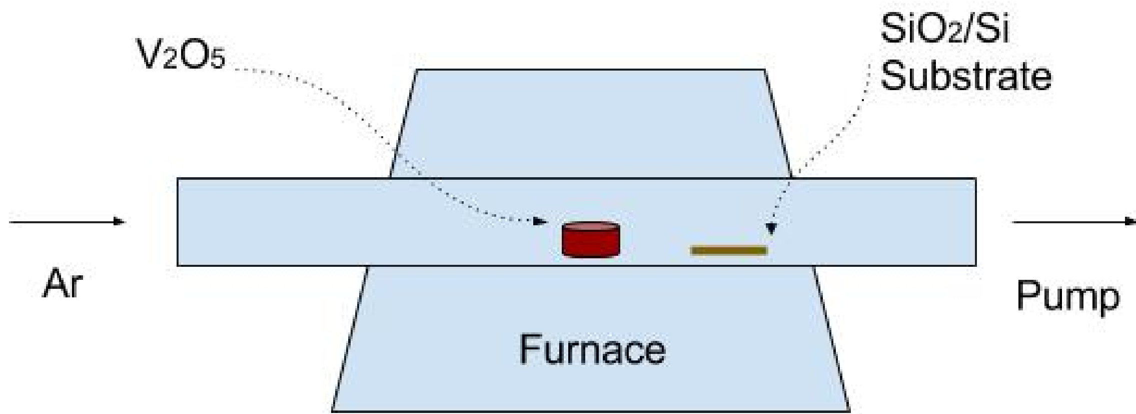

Figure 2.15: VO_2 single crystal nanobeam synthesis diagram

The transferred sample has adhesion with the new substrate. Compared with the original substrate where the VO_2 nanobeams grown, the strain are much less. As shown in Chapter 5, the transition are rather different.

2.3.3 Sample transfer

The VO_2 single crystal nanobeam has a grown temperature $900 \sim 950°C$. This condition makes the VO_2 single crystal nanobeam embedded in the substrate and has a large strain comes from the substrate. A few works[5, 61, 80] has demonstrated that embedded VO_2 single crystal nanobeam has a "poor" transition behavior. To avoid this, we have to transfer the sample from original substrate to a new substrate. By doing this, the strain will be greatly reduced. All our measurement on single crystal VO_2 nanobeam are based on the transferred sample. The Figure 2.17 compared the sample before and after transfer. To transfer the sample, we used PC pick up method.

2.3.4 Lithography

The lithography on VO_2 can only been done by using developer MF319, the developer AZ400K for GaAs will react with VO_2. To work with MF319 developer, we choose

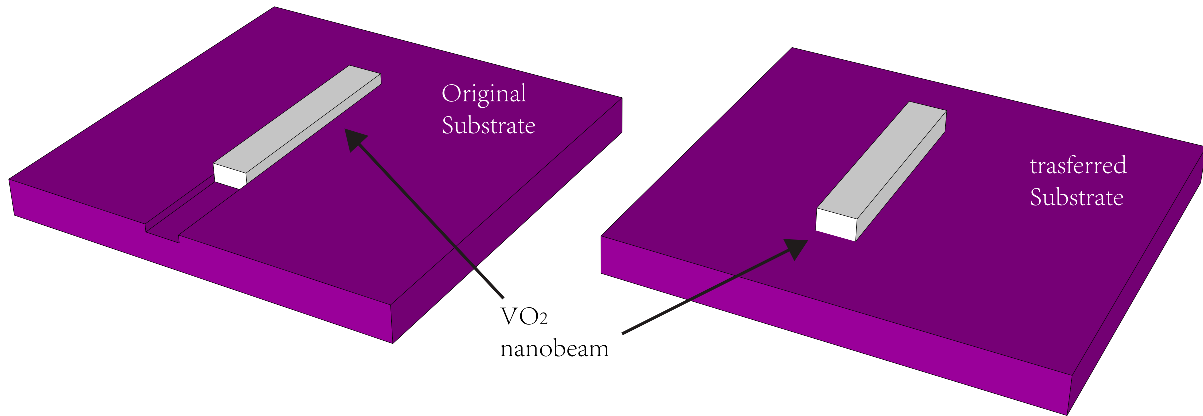

Figure 2.16: Embedded VO_2 nanobeam vs Strain free VO_2 nanobeam

S1811/S1813 as our photoresistor for masking. The thickness of VO_2 nanobeam can ranges from 20nm up to 2μm[30]. In our work, most tested VO_2 nanobeam are chosen to be around 1 μm. Wth this, we need a thicker photoresistor by using slower spin speed. Then soft bake at temperature according to Table 2.1. The following procedures are standard includes: exposure contacts with UV, develop the photoresistor, thermally deposit metal contacts, liftoff.

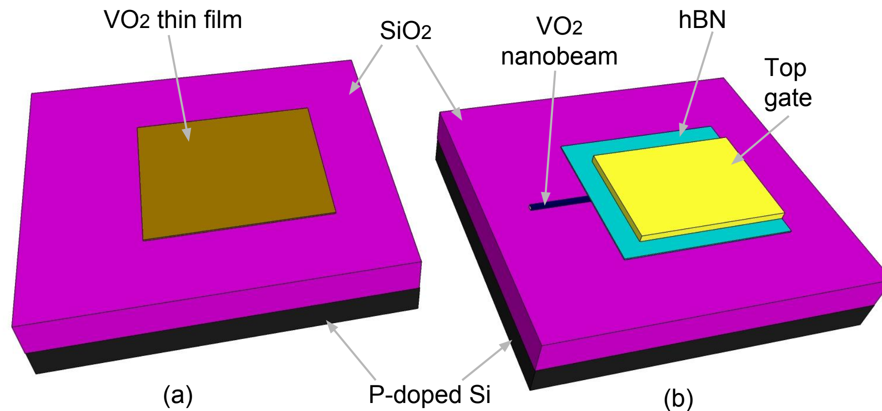

Figure 2.17: VO_2 capacitance sample: a) Thin film VO_2 on Si substrate, the p-doped substrate serves as bottom gate. b) Single crystal VO_2 with top gate and bottom gate.

Another thing to note is depends on the sample surface cleanness, the liftoff are different.

The cleaner the sample surface started with, the easier and better liftoff will be. For those sample surface is not perfect, metal deposition need thinner to ensure the success of liftoff.

CHAPTER 3 Measurement techniques

3.1 Transport measurement

3.1.1 Ohmic contact

After fabrication, next step needs to check if the sample's contacts are Ohmic. When you create a junction between a metal and a semiconductor, some interesting things can happen. The Schottky barrier forms in between the interface, and it may stops the charge carriers to flow easily.

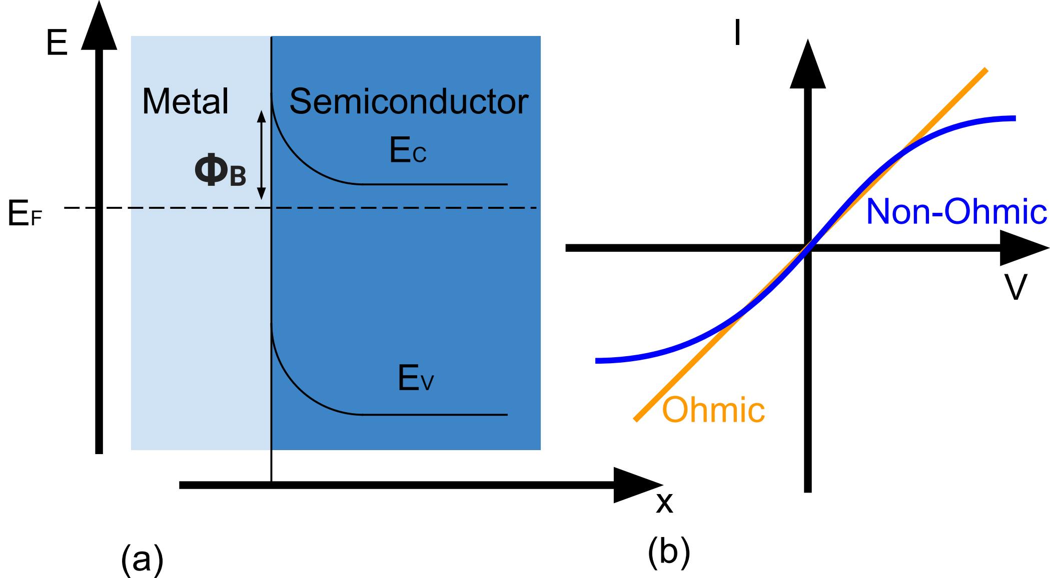

Figure 3.1: (a) Schottky barrier forms between metal insulator junction with a height of Φ_B. (b) Ohmic contact I-V curve(orange) vs non-Ohmic contact I-V curve(blue).

One simple way to test if the juction is ohmic is to measure its I-V characteristics. As shown in Figure 3.1(b), Ohmic contacts shows linear I-V dependence. When it is non-Ohmic, the I-V dependence is non linear. Another way to check if the sample contacts are Ohmic is to compare the resistivity from four terminal measurement and two terminal measurement. Suppose we have four terminal on sample, if two terminal measurement and four terminal

measurement shows same level of resistivity, the contacts are Ohmic. If the two terminal resistivity is much higher, the contacts are normal not ohmic. The validity is illustrated in section below. One advantage of using this method is to protect the sample. Some of our sample are fragile to electrical current. We limit our current to 1nA for protecting these samples. With this small excitation, comparing four terminal and two terminal AC resistivity is more feasible.

3.1.2 Four terminal and two terminal measurement

The mostly used measurement techniques in this thesis is four terminal measurement as shown in Figure 3.2 a, where a current is driven between opposite side contacts while the voltage is measured across two adjacent corner contacts(V_{xx}). The voltage dividing the current yields resistance. Compared with four terminal measurement, two terminal measurement has a source and drain. The resistivity can be obtained using the voltage divide the current going through.

If the sample contact is not good, the two terminal measure result differs from four terminal measurement. Four terminal result is significant smaller than two terminal result. The reason is when performing four terminal measurement, suppose the contacts are bad, the current will not choose to pass though the voltage since they have a higher resistance than the sample bulk. Without current pass though, there is no voltage drop on bad voltage contact. This way the difference of voltage between two voltage reflects the real voltage drop on the sample.

When doing two terminal measurement(Figure 3.2 b) and suppose the contacts are not ohmic. As current is running from 1 to 2, the bad contact makes voltage drop across contacts it self. Then the measured voltage from voltage meter does not reflect the real voltage drop

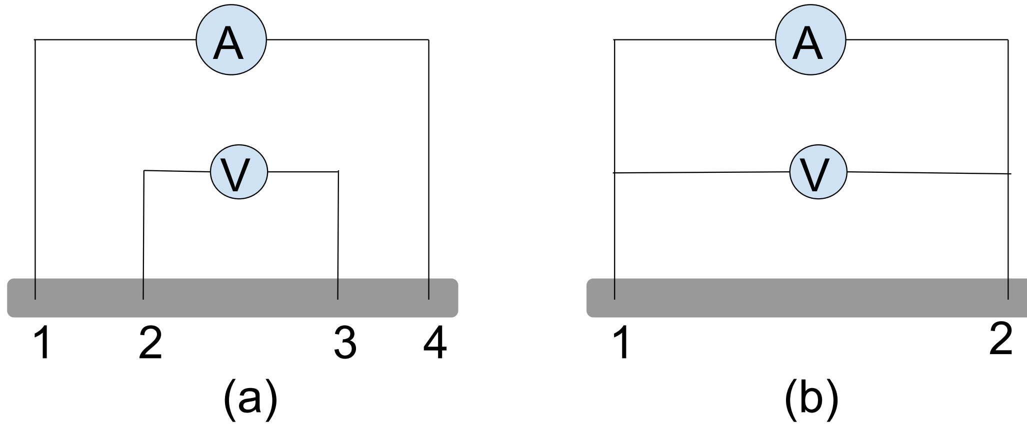

Figure 3.2: Four terminal measurement setup

across the sample.

3.1.3 AC Lock-in amplifier

Lock-in amplifier is a commonly used in transport measurement. It can detect a small signal among tons of noise. Depending on the setup, the lock-in can measure a signal when the noise level is 10^6 times larger than signal level. The principle of lock-in comes from orthogonality of sinusoidal functions.

Assume the noises have signals at frequency f_i, the real signal f_1 together with other f_i multiplied by reference sinusoidal function of frequency f_1 and integrated over a time much longer than the period of the two functions, except f_1 signal , the rest frequencies signals result in zero. Noise is eliminated in this way.

3.1.4 Quantum hall measurement

Quantum hall effect has been discovered in 1971. A detailed description of quantum hall effect can be found in book by Stone[81]. The main idea is: when sweeping magnetic field, the Fermi energy will be tuned through different Landau levels. This makes longitudinal resistivity stays 0 at most time except when the Fermi energy is crossing one Landau level,

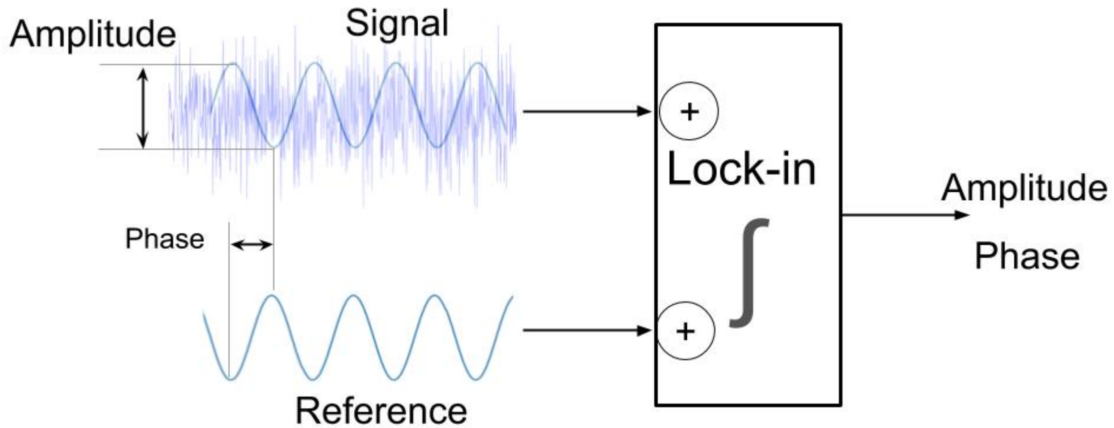

Figure 3.3: Lock-in amplifier

the longitudinal resistivity reflects the bulk behavior. As for the Hall resistivity, it equals to the number of Landau levels lower than the Fermi level times the quantum resistance. It equals to the number of edge channels.

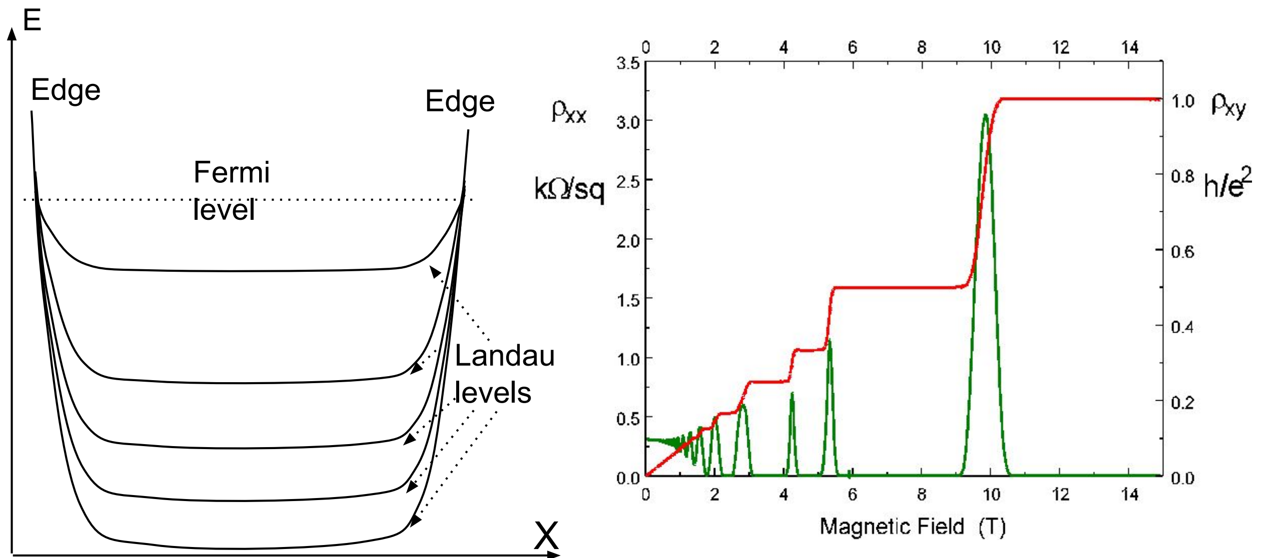

Figure 3.4: Left:Landau levels and fermi energy in a quantum hall system. Right, the longitudinal resistivity and Hall resistivity as function of magnetic field in integer quantum hall effect

The standard setup to do a quantum hall measurement is called Hall bar in Figure 3.5. The current is uniformly applied through the source and drain leads. The longitudinal

resistivity which is the green peaks in Figure 3.4 is measured by monitoring V_{xx} in Figure 3.5. The hall resistivity which is the red plateau in Figure 3.4 is measured by monitoring V_{xy} in Figure 3.5.

When magnetic field is applied, left edge and right edge are both dissipation state, this point, there is no state where the carriers can scatter into, so it appears the same potential on each side. For understand the hall resistivity plateau, suppose the magnetic field is coming out of page in Figure 3.5, electric field is supplied from bottom current lead to top. The Lorentz force makes carriers turns in a way which obey right hand rule. We can easily figure out that the right voltage contacts has the same potential as bottom lead and left has same as top. The conductance between them is through the quantized edge channels. It starts with a lot of edge channels at low magnetic field. As magnetic field increases, Landau levels spacing increases, which led to less edge channels cross Fermi level at edge. As we can see in Figure 3.4, after 11T, the ρ_{xy} reaches h/e^2. The resistivity value h/e^2 is called resistance quantum which is about 25813Ω. One resistance quantum means there is one channel for charge carriers at the edge.

This is the integer quantum hall effect. It can be well understood with the framework of Landau energy splitting and edge channel conducting. An interesting question comes, what will happen if we increase the magnetic field after the hall resistvity already reaches h/e^2?

It turns out into another interesting yet not well understood phenomena which is known as fractional quantum hall effect. Where the number of edge channels turns out to be not integer! As shown in Figure 3.6, there could be 1/3 of channel conducting! What happened? To understand the fractional quantum hall effect, again, we have to consider the correction effect. It is caused by electron-electron interaction together with magnetic flux

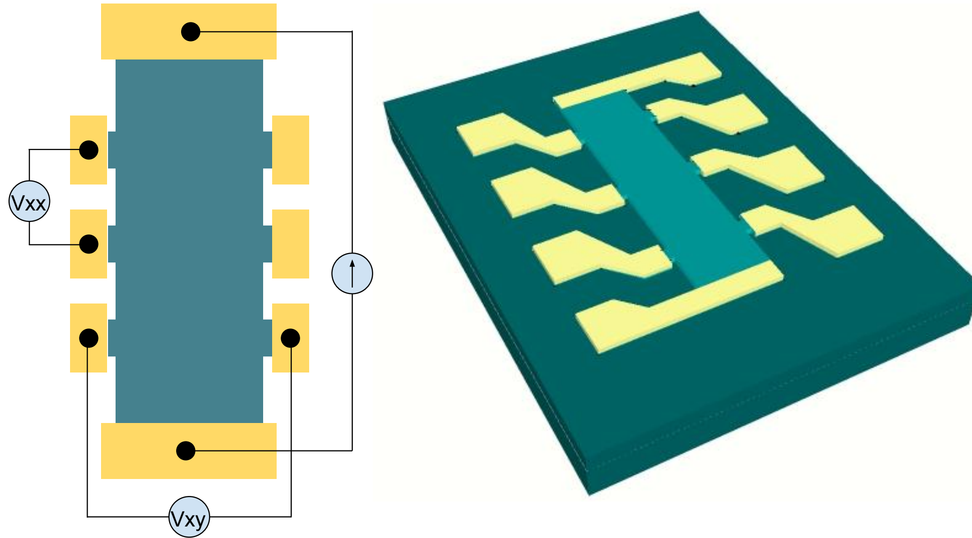

Figure 3.5: Quantum Hall measurement schematic

which forms into composite fermions. This is still not a completely understood area and a lot of active research is still going on. It attracts fundamental research as well as applications. For example, 5/2 state which is known to obey non-abelian particle statistics, is a promising candidate to pave the way to realizing an experimental platform for quantum computing[82]. Details of fractional quantum hall effect is out of the scope of this thesis work. The this work uses integer quantum hall effect to characterize the 2D carriers as well as to drive the carriers into a strong interacting state.

3.2 Low temperature

There are a few cryogenic systems used in this study: Leiden He3/He4 dilution refrigerator; Quantum design PPMS system; Lakeshore flow cryostat. The PPMS system and flow cryostat can goes down to near 3K, which is good to use for pretest sample. Flow cryostat can also be used for high temperature. The dilution refrigerator is used to achieve a temperature of mK range. At which temperature we can measure intrinsic transport behavior of electrons.

Figure 3.6: Fractional Quantum Hall effect.[3]

3.2.1 He3/He4 dilution refrigerator

The Figure 3.7 shows a dry dilution re-fridge system. The system is pre-cooled to 3K with a pulse tube. It takes 2 days to cool down to 3K. This procedure doesn't cost any Helium loss. Then circulation of He3/He4 mixture can cool the lowest plate to 5mK. As shown in Figure 3.7, it is a complicated system with different stages at fixed temperature. The system also has a superconducting magnet on the bottom. The sample is inserted from the top of the fridge. The inserting need to be slow to avoid sudden temperature jump on the sample. Sample has to stay at each temperature stages until fully thermalized before lowing to next stage. The sample measured at mK temperature allow us to do a transport measurement. In quantum hall measurement, the magnetoresistance (ρ_{xx}) and Hall resistance (ρ_{xy}) is measured at a low frequency less than 20Hz. To avoid noise, low pass filter are built on each single line on the probe.

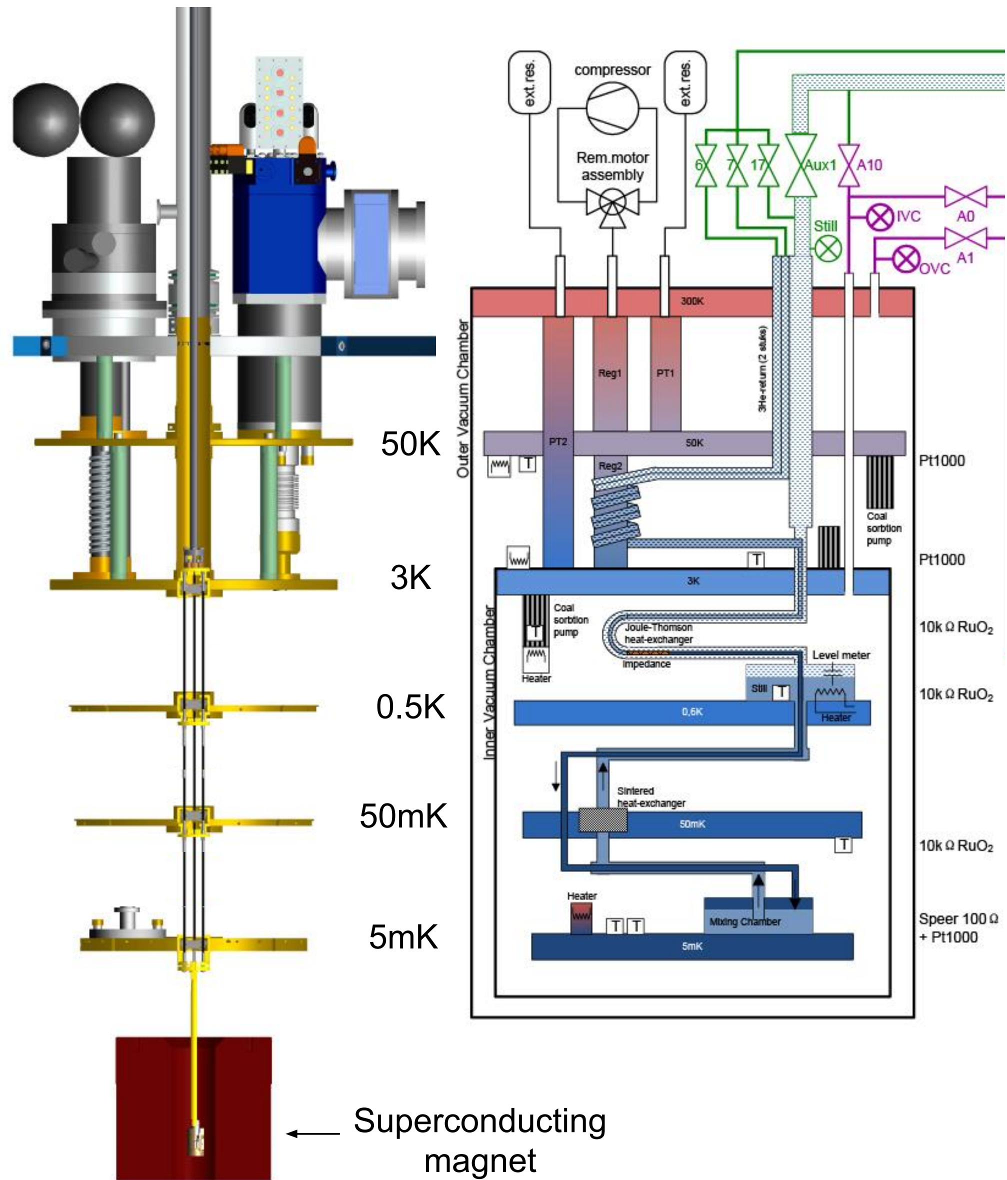

Figure 3.7: Structure of inset of dilution refrigerator with different cooling stage

During last a few years' measurement using dilution refrigerator, we have been improving the cooling power on the sample. Several small methods can significantly lower the sample temperature. For example: using silver paint to glow the sample onto the sample holder instead of vacuum grease; glue the signal cable to the sample holder; gold plate the sample holder surface. Currently used sample holder is shown in Figure 3.8 a. It is made with

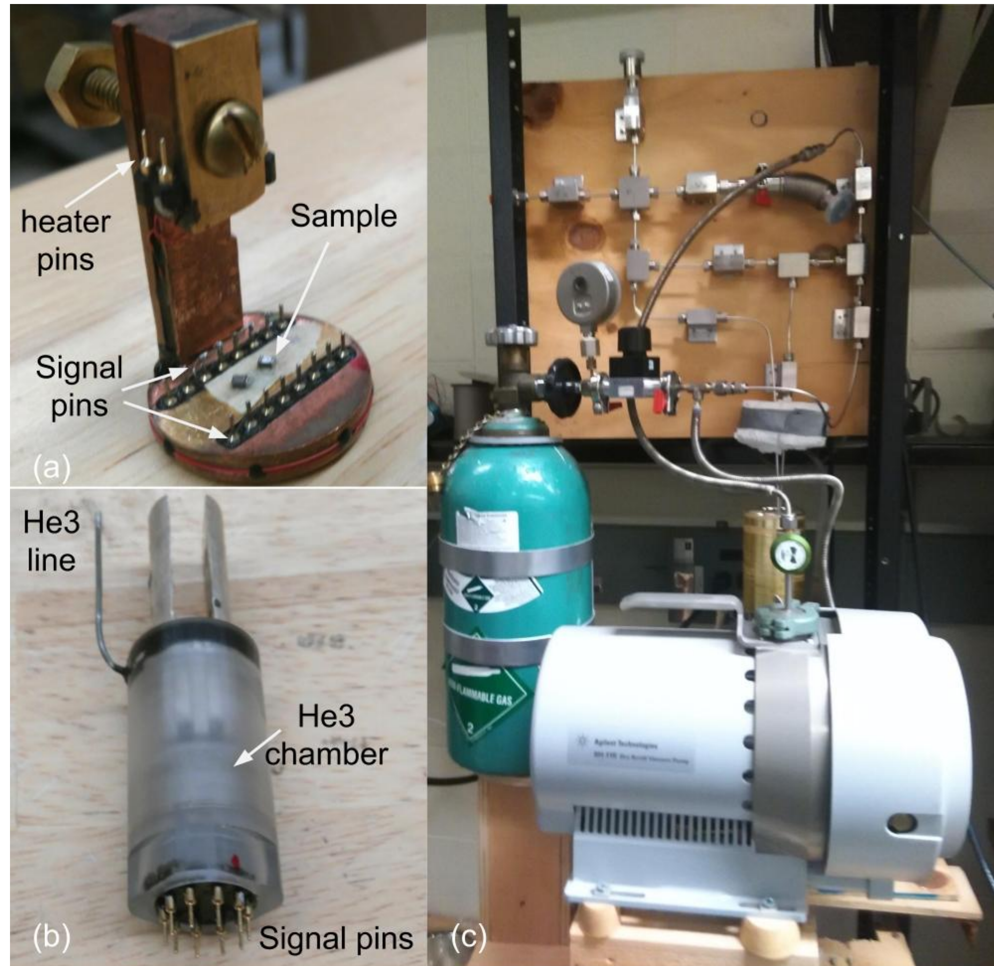

Figure 3.8: a) Currently used sample holder. b) Helium-3 cell sample holder for better cooling purpose. c) Helium-3 cell fillempty control system

copper and critical areas are coated with gold. During the measurement, sample is mount to the sample holder and contacts connect to singal pins on sample holder. This pins finally connects to other connectors on the probe which sends the signal out. The heater pins is

used to run current so the resistive wire(red wire in Figure 3.8 a) can heat up the holder. This is method to probe properties-temperature dependence at mK range. The screw is used to anchor the holder to the end of the probe. A better cooling design is using Helium-3 cell in in Figure 3.8 b. Instead of mounting sample on sample holder. Sample is immersed in helium inside the cell chamber. This way sample is cooled through contacting helium instead of bottom contacting holder. During measurement, the fridge is firstly cooled down to mK temperature. Then the He chamber is filled external Helium 3. To fill the cell and empty, another control system we made needs to be used in Figure 3.8 c. This cooling system is still under test and will serve our measurement in future.

3.2.2 Flow cryostat

The flow cryostat we used in our lab is made by Cryo Industries company. Depends on the coolant, it can be used at liquid Helium temperature as well as liquid Nitrogen temperature. The one we have also can be used above room temperature. During cooling, coolant goes in from coolant inlet and comes out from outlet. The line coolant travels are isolated from main vacuum chamber where sample sits. Although it is designed to use both helium and nitrogen, we rarely use liquid helium due to the high cost. To measure sample at liquid helium temperature, normally we use our dilution refrigerator which is a closed Helium cycle system. Sometimes we also use PPMS which consumes liquid helium in a rather slow rate. Signal feed through can be used to run desired measurement. The temperature use another set of feed through to either maintain at certain temperature or ramp temperature at fixed rate.

The original flow cryostat we bought from company has signal feedthough which is connected with all the twisted signal lines. This is good to lower the noise by reducing the

flux through any possible loops. However, the signal lines are not coaxial lines, they are conducting line covered with insulating material. In our quantum capacitance measurement, using coaxial line for signal is critical. To achieve this, we modified our flow cryostat and implemented four coaxial signal line. In Figure 3.9 a, the alumina window is from the manufacture. We opened four through holes and installed lemo feedthrough. Figure 3.9 b shows the finished parts. These lemo feedthroughs connect to coaxial cables inside vacuum chamber which serves as the signal line.

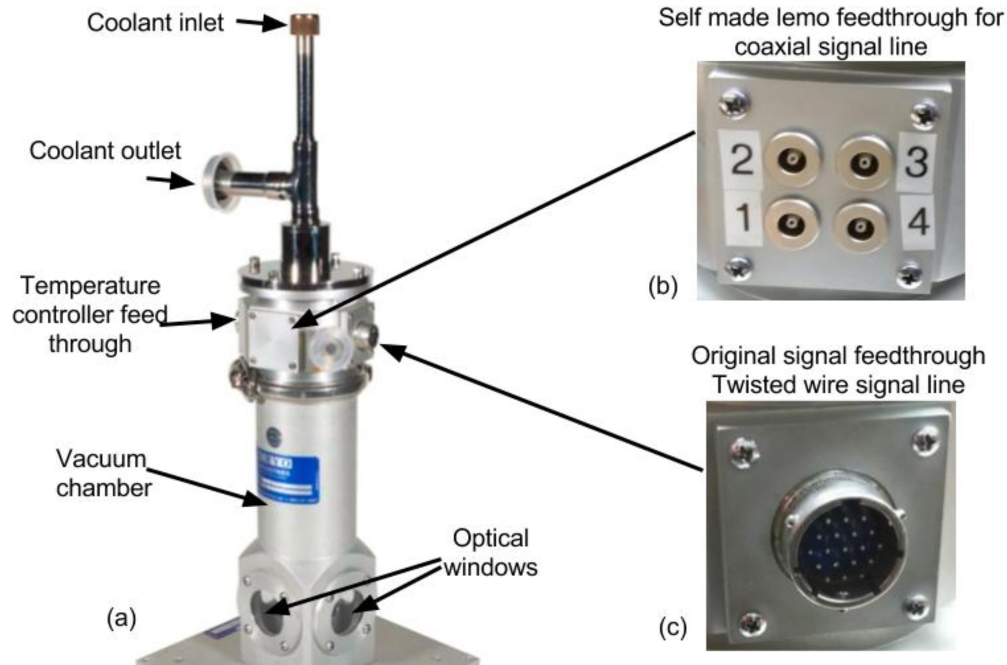

Figure 3.9: Flow cryostat

3.2.3 Physical Property Measurement System PPMS

PPMS is short for Physical Property Measurement System. It is a very popular material characterization system from Quantum design company. It has build-in magnatic field, lock-in, etc. Since the PPMS is a black box system, it's quite easy to learn how to use it. It is also time saving, most measurement can be set in measurement sequence and the

computer will run it automatically. The disadvantage is it's almost impossible to do customized measurement. For example, hall measurement can be done using PPMS. However, the measurement channels are limited. Another drawback is that PPMS has no coaxial line, which makes quantum capacitance impossible. To do customerized measurement, we made a BNC adaptor box which covert the PPMS signal feedthrough pins into BNC connectors and setup the measurement using external instruments.

Figure 3.10: PPMS system

3.3 Quantum Capacitance measurement

Quantum capacitance is first proposed by Luryi in 1988.[31] Normally when we have two metal plates, the capacitance between them is decided by $\frac{\epsilon_0 A}{d}$. This is called geometric capacitance since it only varies with the dimensions of the capacitors. Now, if one of the metal plate is replaced by a semiconductor plane. The capacitance is not simply $\frac{\epsilon_0 A}{d}$. The band structure makes the charging and discharging on the semiconductor plate different as metal plate. There is extra energy that cost by charging or discharging the energy band. This effect makes the real sample capacitance contains two parts in series: geometric capacitance and quantum capacitance. With carefully designed measurement schemes, we can get the

quantum capacitance in our system. There has been reported quantum capacitance in various 2D systems including graphene[83], GaAs[84], LAO[85].

3.3.1 Basic principle

For a normal capacitor, both plates are metals which have infinite density of states. In this condition, we have the simple formula for capacitance. What if one plate becomes semiconductor? Without infinite density of states, charging one plate is not straight forward. Let start with relationship between change of charge and potential[86]:

$$\partial q = C_{Total} * \partial(\mu_{ec}/e) \tag{3.1}$$

Here μ_{ec} stands for electrochemical potential of the electrons. Which is different from chemical potential(Fermi energy). The electrochemical potential is calculated by $\mu_{ec} = eV_{gate}$. Electrochemical potential is the total potential, including both the chemical potential and the electrostatics energy[87]:

$$\partial \mu_{ec} = \mu_c + e\Phi \tag{3.2}$$

In the equation above, μ_c stands for chemical potential, $e\Phi$ stands for electrostatics energy. Now if we plug this expression into Equation 3.1, we will get following:

$$\partial q = C_{Total} * (\partial(\mu_c/e) + \partial\Phi) \tag{3.3}$$

Now rearrange this equation, devide both left hand side and right hand side by C_{Total} and ∂q, we will get:

$$C_{Total}^{-1} = \frac{1}{q}\frac{\partial \mu_c}{\partial q} + \frac{\partial \Phi}{\partial q} = \frac{1}{C_{quantum}} + \frac{1}{C_{geo}} \tag{3.4}$$

3.3.2 Capacitance measurement

Now let's take a look how to extract quantum capacitance experimentally. In several reported systems[83, 85], quantum capacitance are much larger than geometric capacitance. From the Equation 3.4 above, this means the variance of quantum capacitance cause a very small effect on the total capacitance. To be able to measure it, we need to sufficient resolution to capture small changes on total capacitance. Since a large voltage can overrun the chemical potential through electrochemical potential which basically changes the density of states in the system, the most important requirement is to use small signal to run the measurement. Most commercial impedance instrument can easily have a capacitance resolution of smaller than fF. For example, Agilent 4284A Precision LCR Meter can measure capacitance down to 0.01 fF. However, in measuring such a small capacitance, typically it needs an input signal larger than 0.1V and frequency larger than 10KHz to well resolve a capacitor less than 1pF. Therefore, the high voltage signal limits this LCR meter in measuring the quantum capacitance. High frequency also limits the measurement for large resistive sample. The details are shown in Chapter 4.

Ratio transformer bridge

To be able to use a small excitation and still gain enough resolution, the right setup is to use a bridge. We have built three type of bridge for measurement. The first bridge is using ratio transformer, the simplified measurement schematic is shown in Figure.3.11. The left arm has two inductors with tunable inductance with an accuracy of 1E-8 on ratio. The ideal is to tune the ratio between L1 and L2 to null the balance voltage (voltage across middle point of inductors and middle point of capacitors). By doing so, we know the ratio of $\frac{C_s}{Cr}$

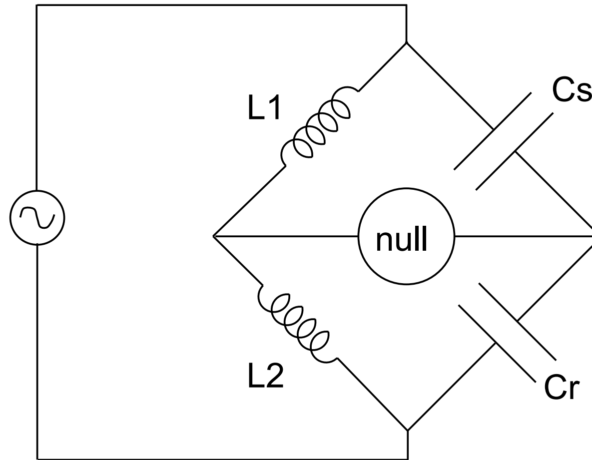

Figure 3.11: Schematic for capacitance bridge.

through $\frac{L1}{L2}$. Capacitor C_r is a standard reference capacitor with fixed capacitance. For the

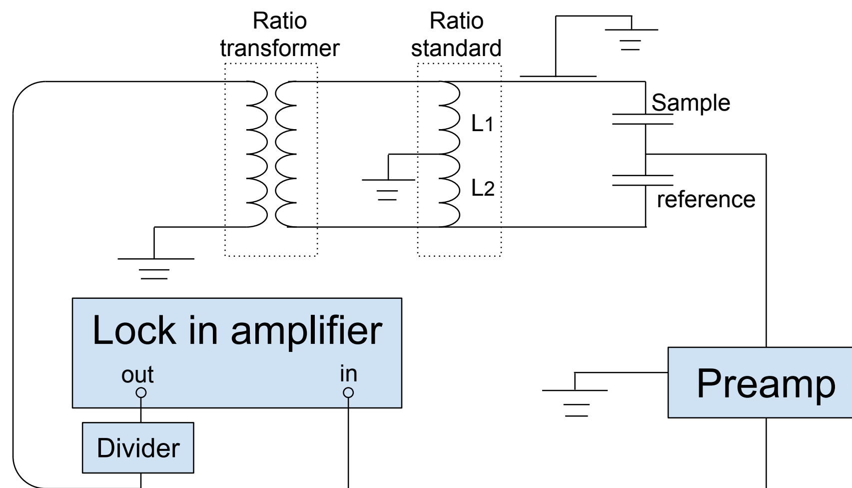

Figure 3.12: Ratio transformer bridge measurement circuit.

real setup, the circuit is complicated than drawing in Figure. 3.11. Figure. 3.12 has more details on the measurement circuit setup. During the measurement, the lock in supplies the drive signal. The divider is used to gain a better signal resolution. The signal is applied to the circuit through a ratio transformer. Notice by using ratio transformer to apply the signal, the measurement circuit and signal drive instrument are using different grounding

setup. For the ratio standard, the balance point is grounded. Then on the right arm of the bridge, the voltage at point between sample and reference is measured relative to ground. It should be close to 0 indicating a balance state.

Balance point can be written as follows:

$$V_b = V_s[\frac{Z_r}{Z_s + Z_r} - \frac{j\omega L_2}{j\omega L_1 + j\omega L_2}] \tag{3.5}$$

In the equation above, $Z_r = R_r - j\frac{1}{\omega C_r}$ stands for reference impedance, $Z_s = R_s - j\frac{1}{\omega C_s}$ stands for sample impedance. If we substitutes these and simplify the equation. We will get the following equation:

$$V_b = V_s[(\frac{C_r}{C_s + C_r} - \frac{L_2}{L_1 + L_2}) - j\frac{\omega C_r R_s}{4}] \tag{3.6}$$

On the right hand side of Equation. 3.6, the first part is determined by sample capacitance, which corresponds to the in phase signal when measuring balance point. The second part is determined by sample resistance which corresponds to out phase signal. Not this result of simplification is based on assumptions: C_r is close to C_s and R_s and $1/\omega C$ is comparable.

During operation, there are two ways to obtain the sample capacitance. First method at each state, adjust the L_1/L_2 ratio to make V_b to 0. Then ratio of $L_1/(L_2 + L_1)$ gives $C_r/(C_s + C_r)$, therefore we can get C_s. However, in the real test, it is not feasible to adjust L_1/L_2 a thousand of times to measure one sample. So normally what we do is balance at one state, and then change the state while recording the balance point. The state can be

changed by external parameters, for example changing tempeatrue of VO_2 can drive it from insulating state to metallic state.

Active bridge

There is one drawback of with a non-zero balance voltage V_b. The validate of derivation is based on the ideal assumption that measuring instrument, preamp has an infinite input impedance. However, in real case, the instrument also has an finite impedance. When V_b is not zero, rather than two components on the balance point, the impedance of preamp also can let current pass through. This effect is not a trouble when Z_s and Z_r is much smaller than Z_m(preamp impedance), which is the situation for polycrystalline VO_2. However, when Z_s is much larger than Z_m, we have to think take this into account. This situation happens when we are measuring capacitance of single crystal VO_2. There are two ways we figured

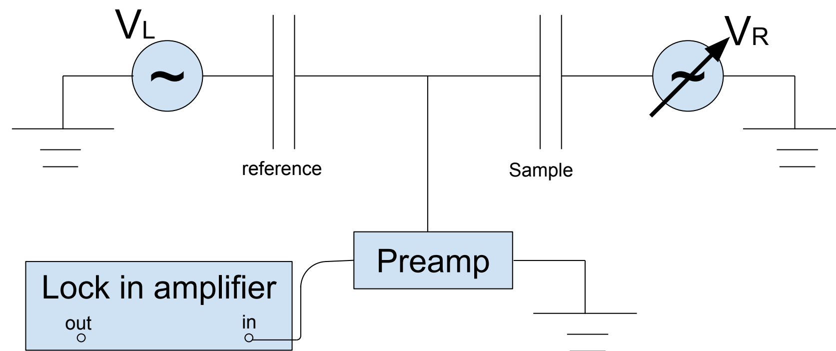

Figure 3.13: Active bridge circuit schematic.

out to deal with this situation. One way is derive the balance point voltage again with considering the instrument impedance term. Then compare it with Equation. 3.6 we can get a correction term. Another way is to keep V_b always at 0V. By doing so, the impedance from instrument is not effect the measurement.

To do so, we need to consider a new bridge setup in Figure. 3.13. Different than ratio

transformer bridge in Figure. 3.12, this setup has no ratio standard. On reference side, there is a signal V_L. On sample side, there is a signal V_R which is 180 degree phase different relative to V_L. With fixed V_L, we can adjust V_R to make monitor lock-in reading go to zero to achieve balance. Once a balance point is reached, we can calculate sample capacitance by using V_L, V_R and C_{ref}. The V_L and V_R are controlled by computer program , and reading from Lock-in amplifier feeds back to computer. The earlier stage of this bridge is shown in Figure. 3.14. The reference signal inputs into two multipliers. The function of multiplier is to multiply the input signal amplitude with a number m between 0 to 1. The accuracy of the m is decided by the digits of the multiplier. For example, the multiplier used in Figure. 3.14 (b) is LTC1650 which has 16 bits. The relative resolution is then $1/2^{16} \sim 10^{-5}$. This means if we have signal of 1V, the relative resolution we have will be 10μV. This is a very high resolution since the capacitance measured is determined by these two signal and the value of reference capacitor. We have successfully tested this setup and can obtain the sample capacitance. In our measurement, we have measured sample capacitance down to 10^{-15}F level.

Later on, we switched Figure. 3.14 (b) to use DDS(direct digital synthesis) functional generator. The differences are: Original one is analog signal and the DDS is digital signal; Original one has 16 bits resolution and DDS only has 14 bits. Although the DDS sacrifices the resolution, it is more noise proof and less electrical hazardous to other instrument.

3.4 Gating and dielectric

In transport measurement, gating has been widely used to introduce external electric field which can change the carrier density in the device. In our work, the gate has been used mostly for capacitance measurement.

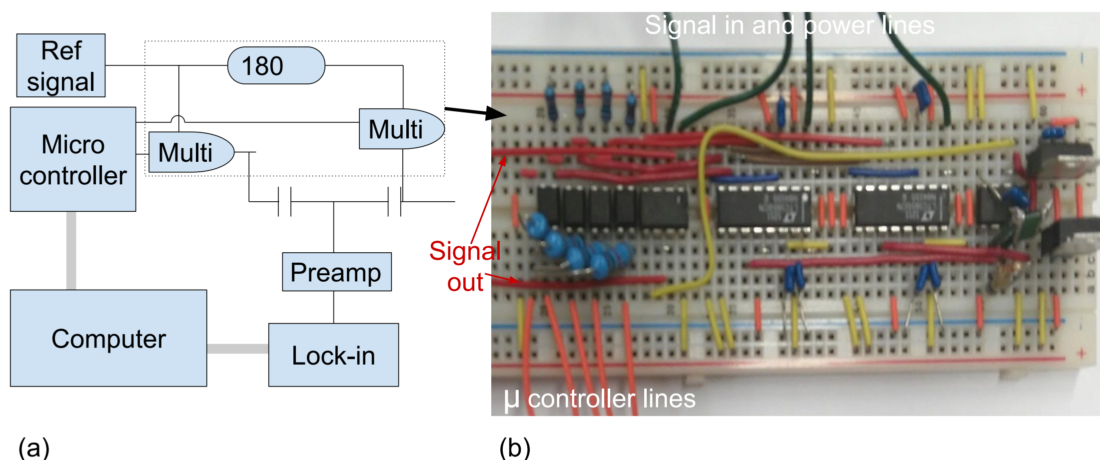

Figure 3.14: Circuit for active bridge. (a) Circuit diagram. (b) The picture of real component of the dotted circled area in (a).

There are two type of gates used in this thesis, the bottom gate and top gate. The bottom gate has been used in both VO_2 thin film and nanobeams. For thin film polycrystalline VO_2 grown on SiO_2 on p-doped Si, the SiO_2 serves as the dielectric layer, heavily p-doped Si as the metal gate. The schematic is shown in Figure. 3.15(a). The SiO_2 has a stable thermal relation, which makes the geometric capacitance formed has a slightly linear decrease with increasing the temperature.

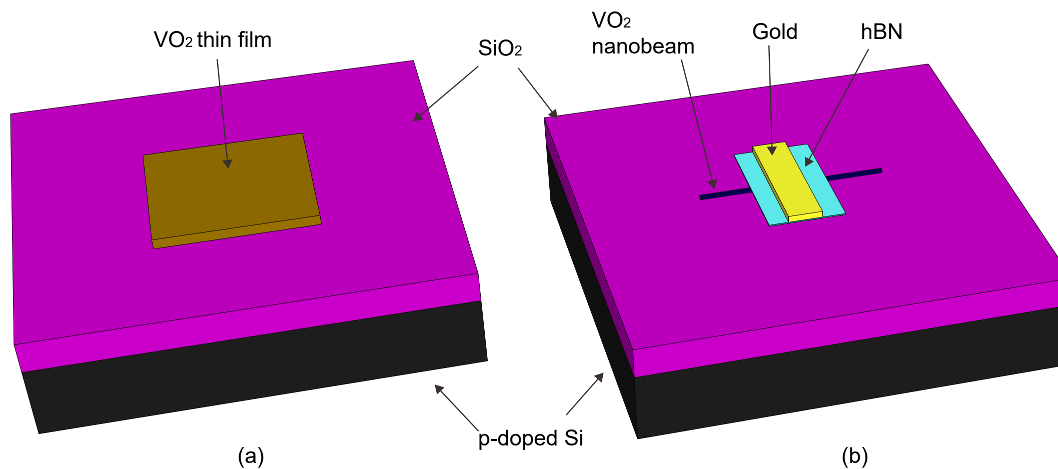

Figure 3.15: VO_2 gating scenario: (a) gating thin film,(b) gating nanobeam

For the top gate method, multi layers of hBN has been used as the dielectric material. The hBN we applied on our sample range from 10 to 20nm thickness. As shown in Figure. 3.15(b), the hBN is on top of VO_2 single crystal nanobeam, another gold contact is deposited on hBN to make a gate. The reason to use the top gate scenario is the sample are rather small compared with the metal contacts. If we want to measure the capacitance between sample and bottom gate, the capacitance will be dominate by the metal contacts area. To be able to resolve this issue, we have to use a top gate and bottom gate together. By grounding the *p*-doped bottom gate during the measurement, the coupling between the top gate and the metal contacts are greatly suppressed.

CHAPTER 4 Study on Polycrystalline VO_2

Part of the result of this chapter have been published in 2014[4].

Metal insulator transition of VO_2 attracts interest due to near room temperature transition and potential applications. The transition of VO_2 is first order which shows discontinuity in the derivative of the Gibbs free energy(G) vs phase parameters(In VO_2 the phase parameter is temperature). The insulator phase and metal phase locates at different local minimum shown in Figure 4.1. Two minimum are in different energy levels. This causes different energy barriers when transit from one to another. In Figure 4.1, from phase 2 to phase 1, the system has to overcome a much larger energy barrier than from phase 1 to phase 2. This explains the resistivity-temperature hysteresis in VO_2. On VO_2 sample studied in this work, when the resistivity is measured as a function of temperature, sweeping up and sweeping down temperature are not in a same trace. This results a hysteresis shown in Figure 4.4.

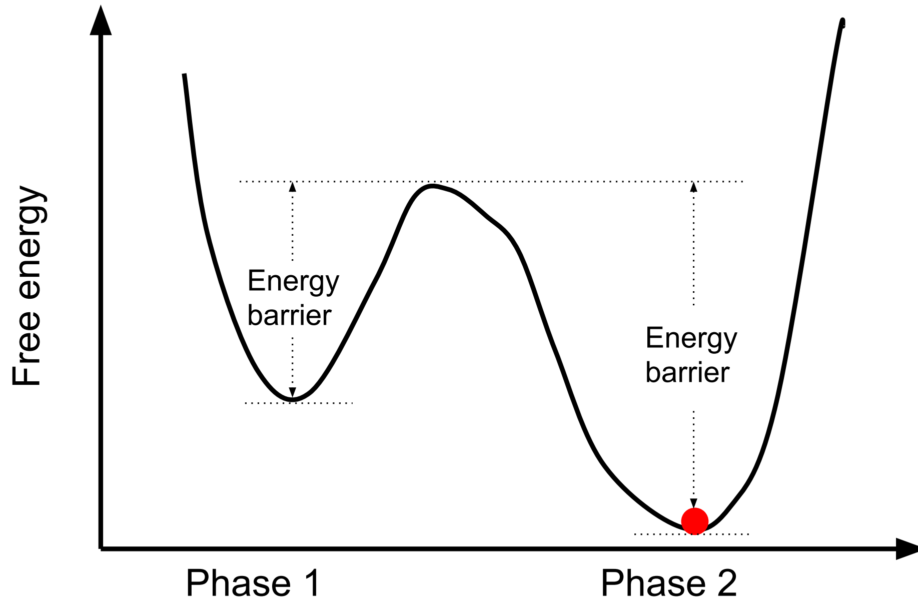

Figure 4.1: Schematic diagram of the free energy as a function of phase parameter.[4]

4.1 Polycrystalline VO_2 characteristics

The polycrystalline VO_2 thin film used in this research is grown on silicon-dioxide/p-doped silicon substrate via pulsed laser deposition. The average thickness of VO_2 in this study is 130 nm. Pulsed laser((10 Hz repetition rate and 350 mJ pulse energy, λ =248 nm)) was used to ablate a metallic vanadium target, the temperature at the substrate was maintained at 595 °C. The other conditions were very similar to those reported previously.[79] Contacts to VO_2 are made by using silver paint. Contacts to the back gate (heavily doped Si substrate with a resistivity 15 mΩ cm) are made by soldering indium at 450 °F. The SiO_2 dielectric thickness is ~285 nm.

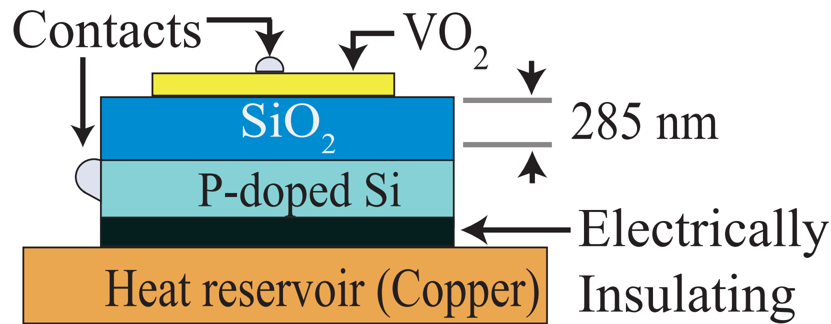

Figure 4.2: Diagram of the polycrystalline VO_2 capacitance device[4].

4.2 Challenges

There are several challenges need to be addressed to characterize quantum capacitance. From introduction part, in order to calculate $C_{\mathrm{q}}(T)$, we need to determine $C_{\mathrm{geo}}(T)$. Normally C_q is large in the metallic regime, which results a smaller contribution to the C_{tot} and is difficult to resolve its variance. Finally, as resistance rises by orders of magnitude, it can easily couple with any stray impedance and distort the capacitance measurement.

Although the commercial capacitance measurement instrument(HP 4284a) can reach a

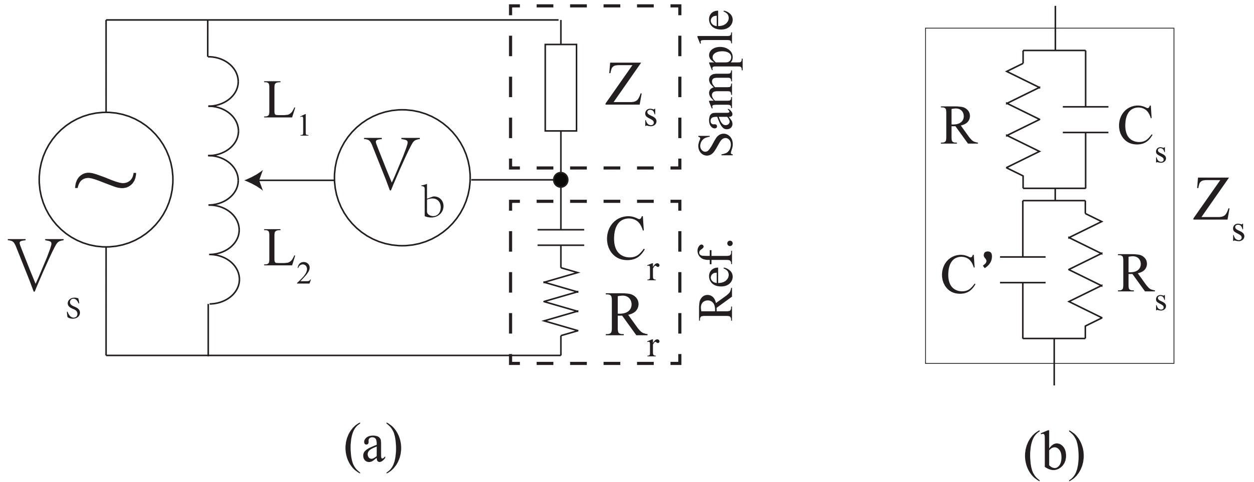

Figure 4.3: (a) Bridge setup (b) Impedance component in the circuit.[4]

resolution down to a few ten Atto fara range, it requires high voltage and large frequency to operate on such a high resolution. Both high AC voltage and large frequency causes issues. The issuses caused by large frequency are explained in 4.3. Since the quantum capacitance resolves density of states(DOS), the high AC voltage applied on sample can capacitively introduce large fluctuation on charge carrier density. Once this fluctuation on density is comparable to the systems's intrinsic charge carrier density, this is no resolution on the band structure. An extreme example will be using too large AC voltage can make the MIT transition happens lower than T_C(340K).

These challenges are overcome by using a homemade bridge capable of resolving capacitance changes to 1 fF (about 0.001% of the total capacitance). Through a careful frequency dependence measurement, we identify not only the geometric capacitance (which varies slightly with T), but also a range of frequencies for which the capacitance measurement is unaffected by the increasing resistance. C_q is then resolved from a finite hysteresis that develops between C_s and C_{geo} in the transitioning and insulating states. We find that

the DOS drops drastically below the MIT, corresponding to the opening energy gap below the transition temperature.

4.3 Measurement Method

A capacitor is formed between VO_2 film and silicon-dioxide/p-doped silicon substrate underneath.[Figure. 4.3]. The SiO_2 dielectric has thickness of 285 nm. Area of the film is obtained from optical microscope, it is roughly 6 mm^2 so expected geometric capacitance is $\epsilon A/d \approx 700$ pF in the metallic regime (Assuming SiO_2 dielectric constant $\epsilon = 3.7\epsilon_0$). Ohmic contacts to the VO_2 are made using small silver paint droplet. Contacts to the back gate are made from indium soldered at the side, which shows a contact resistance approximately 10 Ω. All measurements are performed at high vacuum ($\approx 10^{-5}$ mbar) in flowcryostat chamber isolated from vibration. A PID controled heating loop at rates of 0.1 - 0.3 K/min with resolution 0.01 K. Excellent thermal contact between the substrate and thermal reservoir eliminates T lag at such low ramp rates.

The bridge measurement resolves resistance and capacitance as shown in Figure. 4.3(a). Before each measurement, we ramp the sample to high temperature($T = 360$ K) where the VO_2 is in metallic state, and bridge is balanced by adjusting the components L_1, L_2, R_r and C_r. After balancing, R_r and C_r are then fixed and held at room temperature. $V_b(T)$ is measured as the sample undergoes a thermal cycle.

The goal is to resolve the quantum capacitance by accurately measuring sample capacitance C_s and VO_2 sheet resistance R_s by monitoring the balance point voltage V_b. Under certain conditions, changes in C_s stands for the real part of balance voltage, and changes in R_s appears in imaginary parts of V_b. For this measurement, one challenge is that R_s has a few orders of magnitude changes, at high frequency since the impedance are closer to each

other, this can easily overrun the sensitivity to C_s even for a small amount of mixing between $\mathrm{Re}[V_b]$ and $\mathrm{Im}[V_b]$. Now let's take a look how to avoid mixing by choosing appropriate measurement frequencies.

The sample total impedance model Z_s is shown in Fig. 4.3(b). There are totally four components forms Z_s, in addition to C_s and R_s, the SiO_2 dc resistance R, and the capacitive coupling C' between different points of the film ($C' \lesssim C_s$ occurs mostly through the gate) have been included. Frequency f must be large enough that capacitive coupling is much greater than conduction through the dielectric, yet small enough that the signal-induced in-plane voltage drop across the VO_2 remains negligible compared to the gate potential. Impedance Z_s then simplifies to a capacitor with equivalent series resistance (ESR) $Z_s \approx R_s + (i\omega C_s)^{-1}$. Under these conditions,

$$V_b \approx V_s \left[\left(\frac{C_r}{C_s + C_r} - \frac{L_2}{L_1 + L_2} \right) - i \frac{\omega C_r R_s}{4} \right]. \tag{4.1}$$

This greatly aids the data analysis since C_s and R_s are separated into the real and imaginary components of V_b, as described above.

Finally, the terms of Eqn. 4.1 are inverted to express C_s and R_s. The film resistance is $R_s = -4\mathrm{Im}[V_b]/\omega C_r$. In the present sample geometry, it would be difficult to accurately convert R_s to resistivity, so this has been left as an extrinsic parameter in the results. For the small capacitance changes observed [$\mathrm{d}C_s/\left(C_s|_{360\ \mathrm{K}}\right) \approx 0.05\%$], $\mathrm{Re}[V_b]$ is linearly proportional to changes in C_s:

$$\mathrm{d}C_s = C_r \frac{(1-x)^2}{V_s} \mathrm{Re}[V_b] \tag{4.2}$$

where $x = L_2/(L_1 + L_2)$ is set to seven digits accuracy by ratio transformer. This proportionality constant is obtained from the Taylor expansion of Eqn. 4.1 with respect to C_s. Below, the decoupling of Re[V_b] and Im[V_b], the independence of Re[V_b] on f, and the linear f dependence of Im[V_b] are all used to identify the range of f for which Eqn. 4.1 is valid.

4.4 Results

Figure 4.4 demonstrates Resistance measured by using 2-terminal probe method(green line) has a very good agreement with resistance extract from bridge. excellent agreement between R_s obtained using the bridge and results from a 2-terminal in-plane measurement R_{2t}. Consistent with previous findings [88], both configurations demonstrate a hysteresis ranging from about 335 K to 350 K where resistance changes by several orders of magnitude. Compared to single crystal results [25, 61], this transition is somewhat smoothed by the film's polycrystalline structure [Figure 4.4]. The bridge measurement is performed at several frequencies ranging from 15.5 Hz to 185.8 Hz. Figure 4.5 confirms the linear relationship Im[V_b] $\propto f$. These findings support the above analysis leading to Eqn. 4.1.

The ability to resolve changes in C_s as distinct from R_s depends on the amount of mixing between Re[V_b] and Im[V_b]. Figures 4.6(a) and 4.6(b) display both signals Re[V_b] and Im[V_b] as functions of T [note the change in units from (a) to (b)]. For larger f, the real and imaginary traces have almost the same shape, indicating that f is outside the range for which R_s and dC_s can be decoupled as discussed above.

Figure 4.6(c) confirms that sensitivity to dC_s is overrun by changing film resistivity at 87.8 Hz and 185.8 Hz, where Re[V_b] is nearly a single valued function of Im[V_b]. However, slightly decreasing f is sufficient to decouple Re[V_b] and Im[V_b] as demonstrated in the inset. For traces below 30 Hz, Re[V_b] changes by up to 80% at fixed Im[V_b], is non-monotonic, and

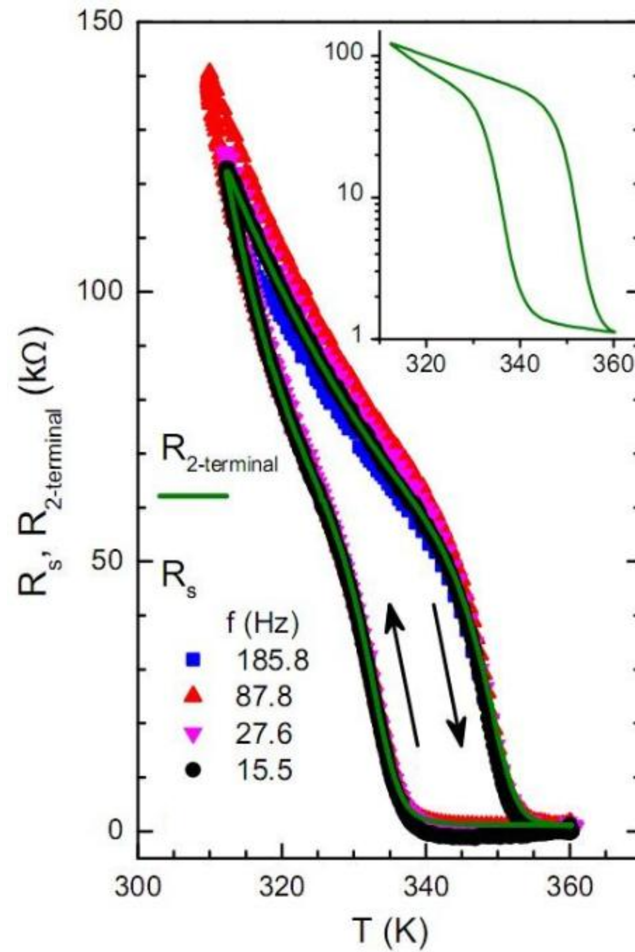

Figure 4.4: Comparison of standard in-plane 2-terminal technique (green line) with bridge technique (scatter plots) for measuring sheet resistance. Arrows distinguish between heating and cooling cycles. The in-plane measurement is shown on a semi-log plot in the inset.[4]

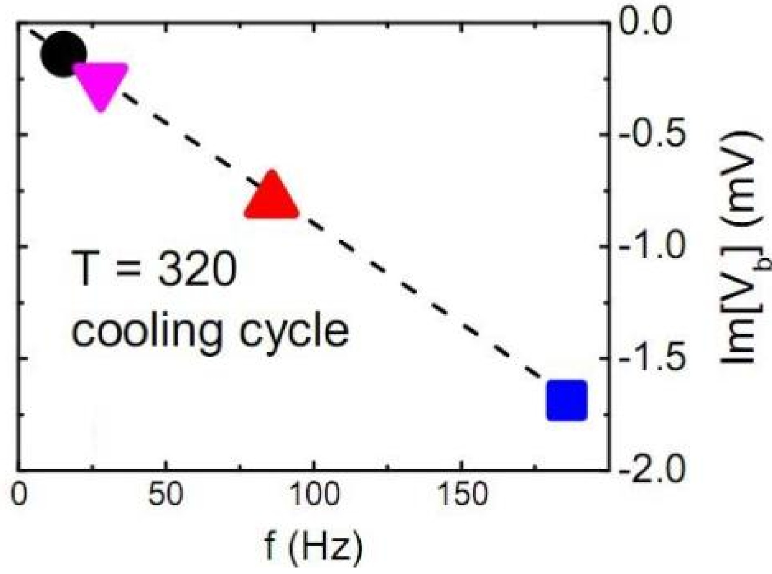

Figure 4.5: Confirms linear relationship $\mathrm{Im}[V_b] \propto f$ from Eqn. 4.1.[4]

lies completely within a region where even the high-f measurements are relatively independent of $\mathrm{Im}[V_b]$. Thus, the low-frequency trace allows capacitance changes across the MIT to be resolved without significant distortion by the changing film resistivity.

Figure 4.6(d) displays the capacitance changes dC_s calculated from the data in panel (a) according to Eqn. 4.2. Regardless of f, all traces collapse onto a single curve in the metallic regime where $C_s = C_{\mathrm{geo}}$. This allows the smooth T-dependence of C_{geo} to be identified and extrapolated below the MIT as a dashed line. In this region, the 15.5 Hz and 27.6 Hz measurements overlap nearly perfectly. For this range of f over which C_s is frequency independent, Eqns. 4.1 and 4.2 are validated.

Figure 4.7 focuses on the 15.5 Hz result from above. Panel (a) reproduces the data from Figure 4.6(d) with estimated geometric contribution (dashed line). To both has been added a constant, the total capacitance measured at the balance point, $C_s^{360\ \mathrm{K}} = 693.1$ pF. Dotted error bars indicate uncertainty in V_b, which drifts up and down within a narrow range on

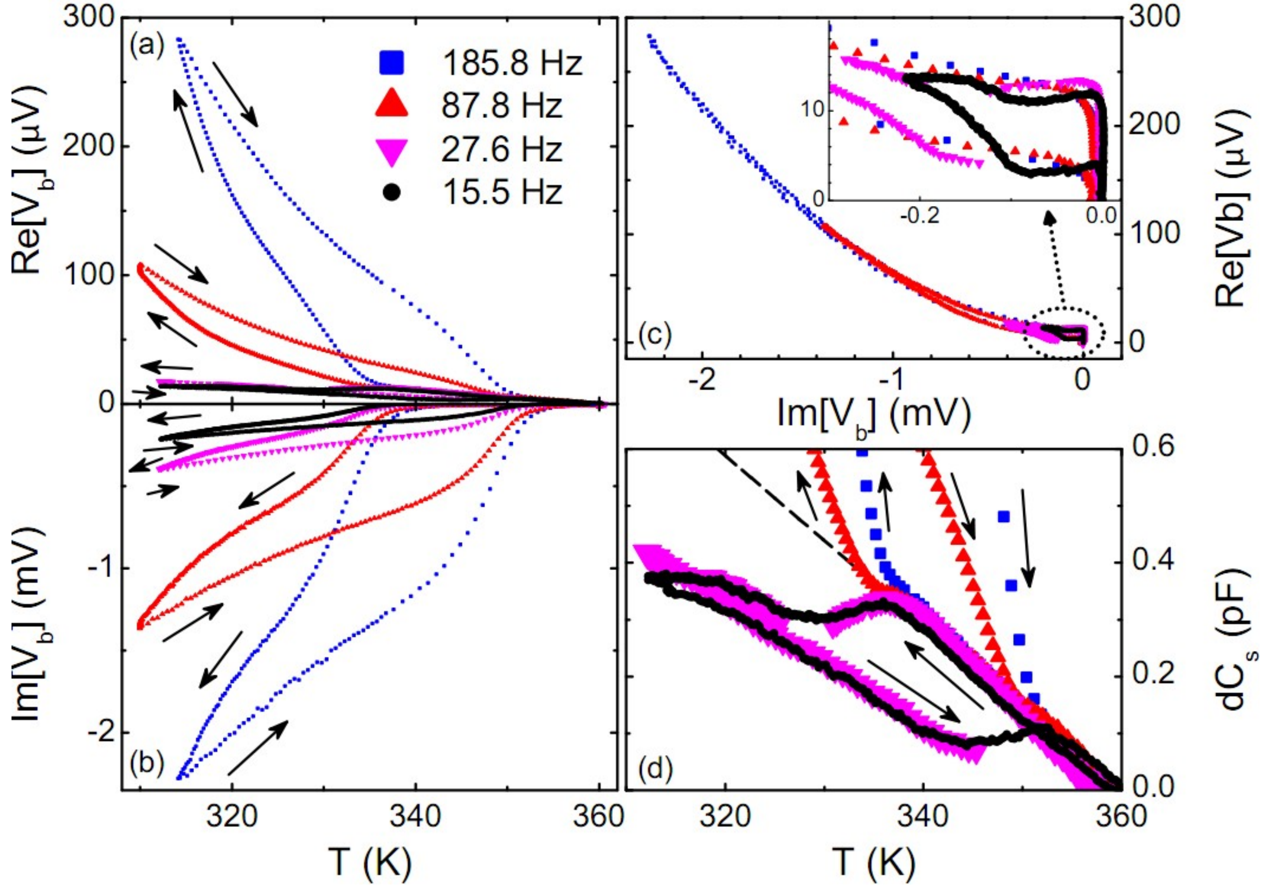

Figure 4.6: (a),(b) Re[V_b] and Im[V_b] as functions of T. Note the change in scale from μV to mV. (c) Re[V_b] as a function of Im[V_b] is a monotonic nearly single-valued function for high frequencies. Inset highlights low frequency measurement where mixing is eliminated. (d) Capacitance changes dC_s as a function of T. The slope of all traces in the metallic regime gives the T dependence of $C_{\rm geo}$ which has been extrapolated below the MIT as a dashed line.[4]

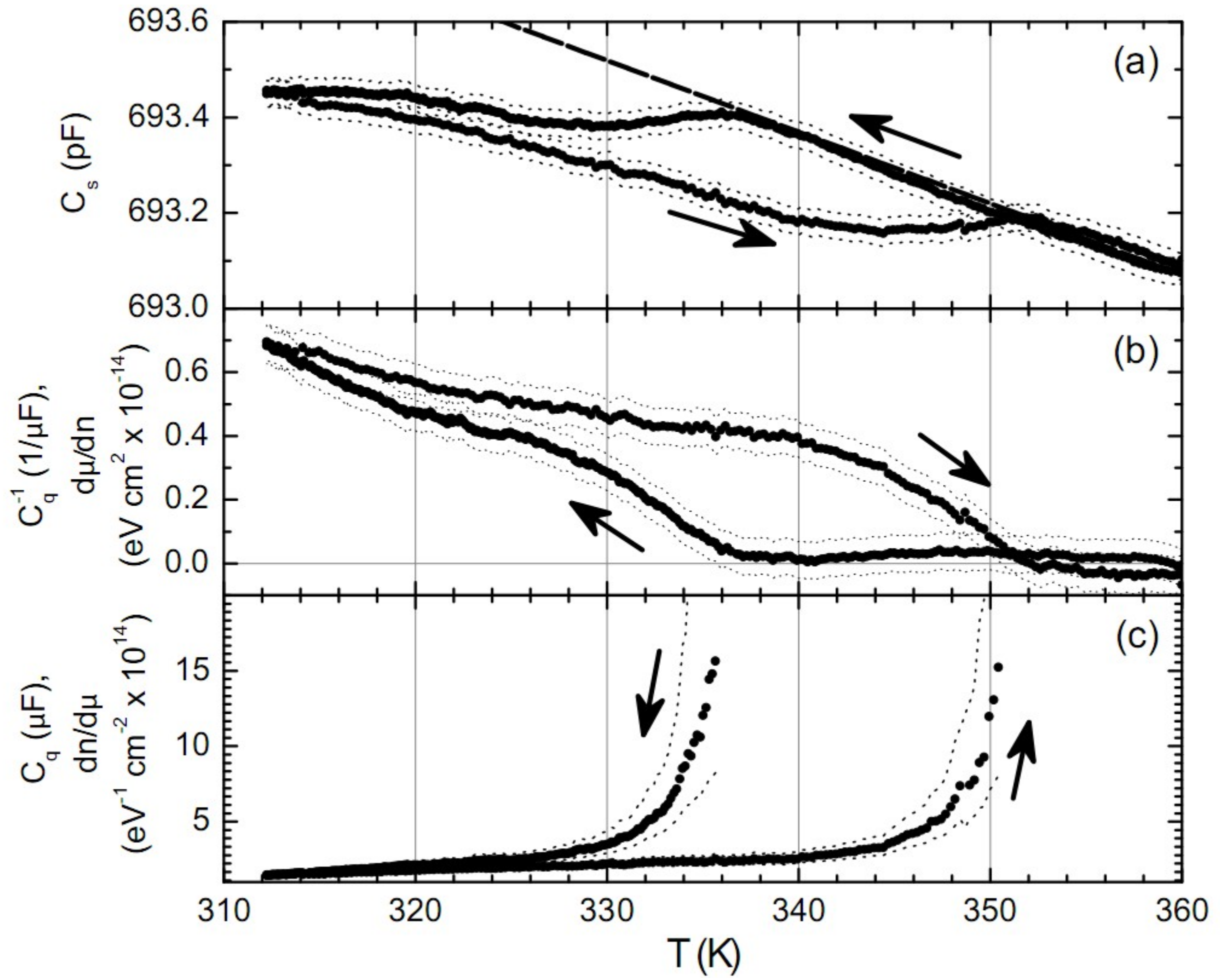

Figure 4.7: (a), (b), and (c) C_s, C_q^{-1} and C_q as functions of T. In (c), only a portion of the thermal cycle is shown, since larger C_q cannot be resolved. [4]

the time scale of a few hours or more when the sample is at fixed temperature. This is much smaller than the observed hysteresis, and only affects our ability measure the sign of C_q in the metallic regime [as shown in panel (b)]. Panels (b) and (c) display $\mathrm{d}\mu/\mathrm{d}n$ and $\mathrm{d}n/\mathrm{d}\mu$ with the associated uncertainty.

Figure 4.7(b) demonstrates the finite energy cost for charging the film by amount $\mathrm{d}n$ during a charging cycle. For this measurement, $\mathrm{d}n = 3 \times 10^9$ cm^{-2} is 3 or more orders of magnitude less than than the carrier density n (discussed below). The charging energy [at most $(\mathrm{d}\mu/\mathrm{d}n)\mathrm{d}n = 6$ meV or 70 K] is then a small perturbation of the system, far less than the thermal energy at the MIT. Though clearly positive in the insulating regime, the sign of $\mathrm{d}\mu/\mathrm{d}n$ becomes difficult to determine as the metallic state is approached. To increase the resolution of C_q requires much thinner, high quality dielectric which is experimentally difficult to achieve. Thus, the possibility of negative compressibility $\kappa = n^{-2}\mathrm{d}n/\mathrm{d}\mu$, a signature of strongly correlated charges previously observed in other systems [84, 85], requires further investigation.

Figure 4.7(c) displays the DOS on a linear scale over the range for which sign($\mathrm{d}\mu/\mathrm{d}n$) can be determined. With increasing T the DOS grows very large, as expected for metal. Below the MIT, $\mathrm{d}n/\mathrm{d}\mu$ shows only slight temperature dependence. The slope changes abruptly at the transition point and cannot be fit to a power-law or exponential dependence on T. In fact, the concave of the slope changes sign from positive to negative upon cooling, suggesting a cross-over between different mechanisms at the transition.

CHAPTER 5 Study on Single crystal VO_2 nanobeam

5.1 Background

The synthesis and characterization of VO_2 single crystal nanobeam has been firstly reported by Park's group[5]. Compared with polycrystalline VO_2, the metal insulator transition in single crystal VO_2 are rather abrupt. It is more like a step function(Figure.5.1 b) when resistance is measured as a function of temperature. The abrupt transition comes from its single crystal nature. To understand it, we need to take a look why polycrystalline VO_2 has a smooth transition. The smoothed transition on polycrystalline VO_2(Figure.4.4 inset) is due to its multi-grain structure. Although all grains favor at same transition temperature, they are in different shape and size and are surrounded by other grains. The build in strains for each grain of VO_2 are different. Several studies have shown this can be an significant effect on MIT behavior for VO_2[6, 61, 80]. Polycrystalline VO_2 contains numerous sizes of grains. The observed transition on it is due to the averaged effect. As for single crystal VO_2, the single crystal phase yields should yield one transition. This is the reason why the transition on single crystal VO_2 is similar to a step function.

Several studies have been done to study the transition mechanism of single crystal VO_2. Resistance measurement[30, 61] has revealed the strain plays an important role in the metal insulator transition. Following research has demonstrated by engineering the strain on VO_2 nano beam[6], the transition can be controlled. Optical measurement from Ruan's group[25] has demonstrated the structural phase transition and Mott transition have different transition temperature and can be well separated. The Mott induced transition shows no hysteresis and structural phase transition has a hysteresis. Several groups have reported the gating of VO_2 single crystal nanobeam[89, 90]. One scenario[90] is atomic layer deposition of 20

nm high-K deictic material. This method provides an electric filed of 10^8V/m. With this large electric field, the resistivity of single crystal VO_2 changes about 10%. This again demonstrated the notorious hardness of gating VO_2. Another scenario of gating uses ionic liquid[91] has demonstrated a significant transition(two order of magnitude) by tuning the electric field.

Although much have been done to study single crystal VO_2, transport measurement is mostly focused on resistivity measurement. Non measurement has revealed it electronic structure. Our work here is aiming at resolving its electronic structure by using quantum capacitance measurement. Before we go there, we take a look at Characteristics of single crystal VO_2 and some other effects we have observed.

5.2 Single Crystal VO_2 Characteristics

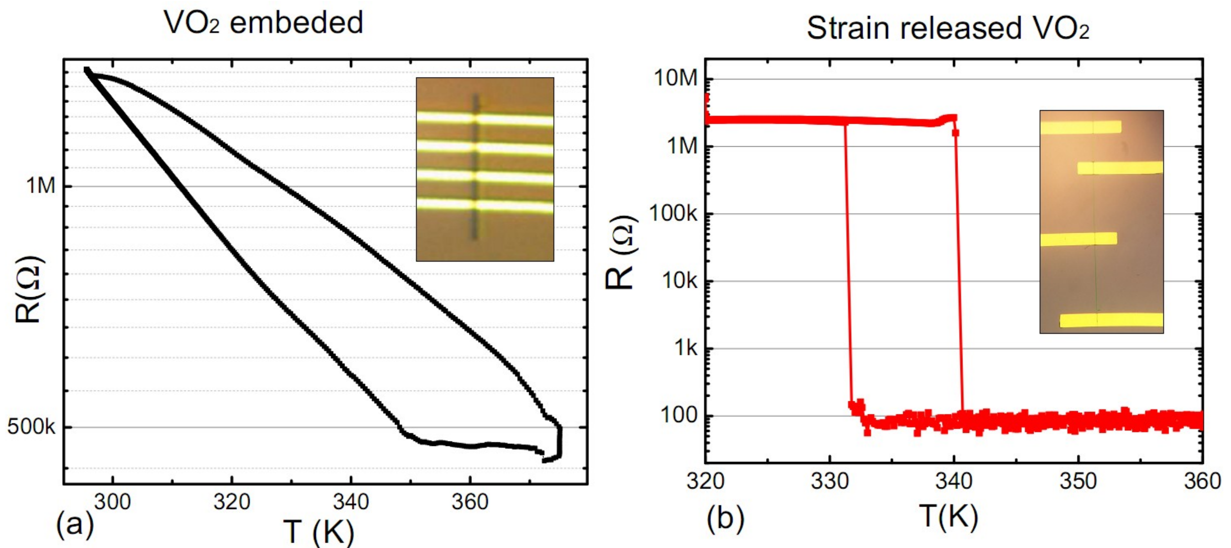

Figure 5.1: Left:Resistivity measurement on strained VO_2 on substrate; Right: Resistivity measurement on strain free VO_2

As mentioned, strain plays an important role in VO_2 MIT, Figure 5.1 shows the transport measurement on strain free VO_2 comparing with strained VO_2. Single crystal VO_2 embedded

into the SiO_2 substrate during the growth, this introduce an tremendous build in strain.[61] The single crystal VO_2 is grown on [100] direction, which also corresponds to the lattice C-axis.[61] As shown in Table 1.3.1, at high temperature, C_R=2.86 $\AA$ compared with low temperature C_{M1}=5.75 $\AA$. At low temperature monoclinic, each unit cell contains as twice atoms as high temperature rutile phase. Consider these together, the sample has about 1% changes along its C-axis. For SiO_2, the thermal expansion coefficient is 0.55-0.75$\times 10^{-6}$/K. At the temperature range from 300K to 360K, SiO_2 stays almost same length compared with VO_2. This mismatch cause an tremendous external force to hold VO_2 through the adhesive interaction between the nanobeam and the substrate. To reduce the strain, after growth, VO_2 is mechanically transferred onto a new substrate(see Chapter 2). Although the Van der Waals force still exists after VO_2 transferred to new substrate, it has been proven orders smaller than the strain caused by embedding[30]. The strain free single crystal VO_2 demonstrates a change on resistivity larger than 4 orders and the transition happens within a quite narrow temperature range $< 0.1°$C(Figure 5.1.b). In fact, it happens so quick that it resembles a step function. Compared with strain free single crystal VO_2, Figure 5.1.a shows measurement on a single crystal VO_2 embedded in the SiO_2. The MIT is observed, it also shows hysteresis(Red curve for heating, blue curve for cooling). However the resistance trace are not smooth. This is a poor transition even compared with polycrystalline VO_2. Further study has been done to investigate the stain effect on single crystal VO_2 nanobeam.[61, 80] Figure 5.3.a shows at 373.15 K, nanobeam exhibited a striking periodic bright dark pattern. The pattern can persist between $\sim$ 343K and $\sim$ 423K. This pattern can exist in a large range of temperature is due to the strain comes from the substrate. The periodic bright dark pattern configuration represents the lowest-energy the system can reach by balancing

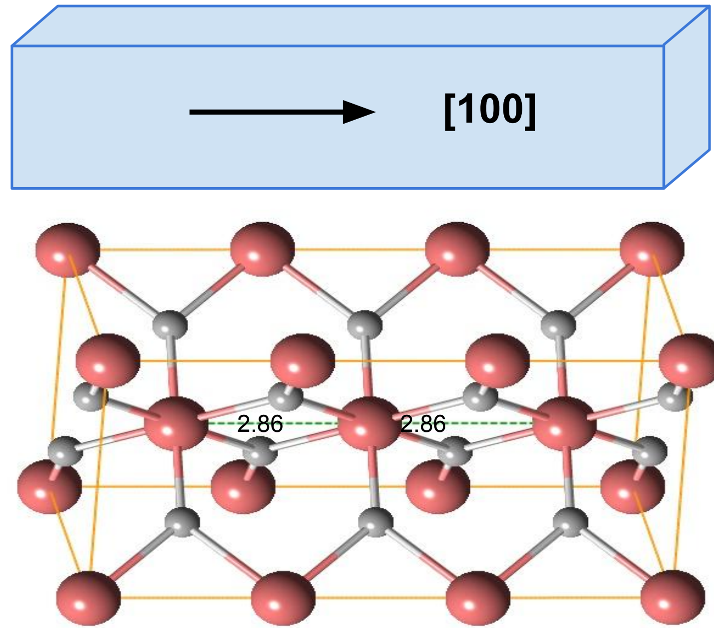

Figure 5.2: Growth direction of Single Crystal VO_2

between the elastic energy and the domain wall energy.

5.2.1 Ohmic Contact

Ohmic contact is always important to start a good transport measurement. As for VO_2, the Ohmic contact to polycrystalline VO_2 is straightforward. So far, we have achieved ohmic contacts using different type of metal(Cr+Au, silver paint). For single crystal VO_2 nanobeam, the contacts can easily degrade after a few thermal cycles since the sample itself undergoes shrinking and expanding during the thermal cycles. This weakens the metal attached to it. The thicker metal, the harder for the contacts to degrade. This is why several published works[30, 61, 92] use a few hundred nano meters thick contacts. Silver paint and indium also have proved to be effective contacts. However, the quality is not as good as metal deposition.[92]

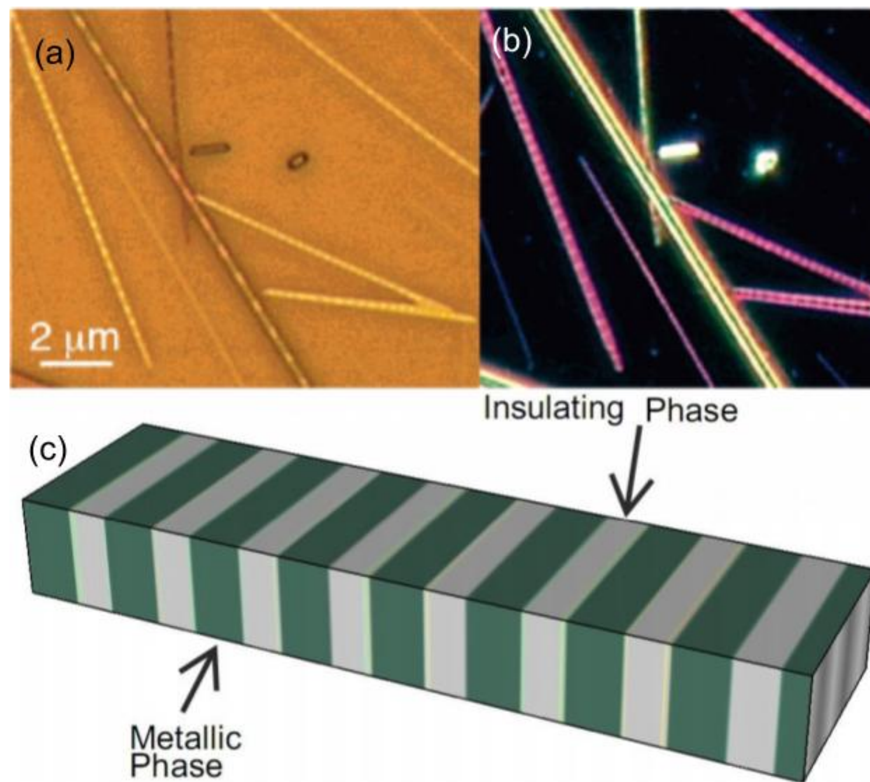

Figure 5.3: a), b)Optical image of single crystal VO_2 near transition temperature shows different color alternating strips.[5] c) Schematics of insulating metallic alternating stripes.

5.3 Strain effect

Unlike polycrystalline VO_2, single crystal VO_2 suffers a lot from strain effect. The Figure 5.1 shows the resistivity-temperature dependence difference between strained and strain free single crystal VO_2. This may cause some problems in our capacitance measurement as shown in latter sections. In fact, the strain effect is so tremendous that it has been used as a method to engineer metal insulator transition in VO_2. Since the single crystal VO_2 has a very good mechnical properties, the external force can be applied on it without breaking it. In our test, we have bent single crystal VO_2 beam into 180 degrees with an arch radius of 10 μm. In Figure 5.4, Wu's group has demonstrated using uni-axial external stress to engineerly create insulating domains along single-crystal beams of VO2, and to observe the transition at room temperature.

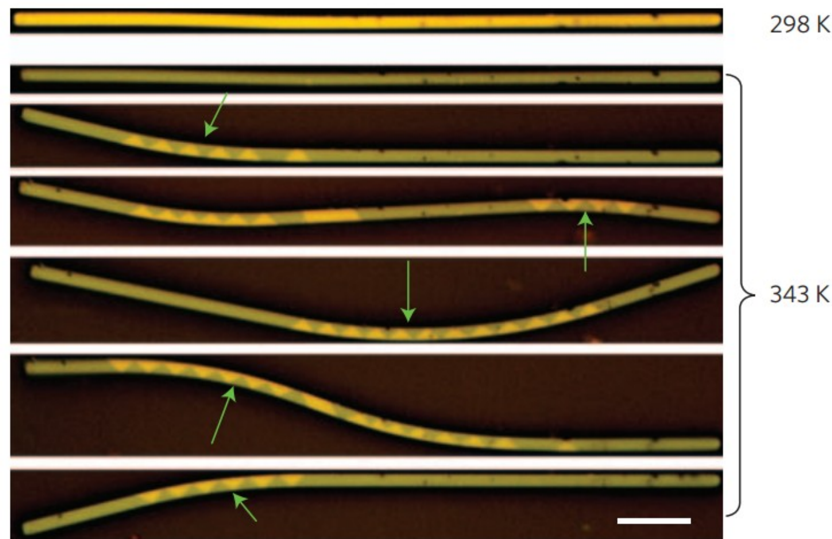

Figure 5.4: The green arrow indicating the direction of external force applied by tungsten needle. The orange color is the insulating domain.[6]

5.4 Light effect

Light effects on VO_2 has been studied for many years[7, 93–98]. Most research works focus on using infrared laser to make VO_2 undergoes transition[96–98]. The power intense laser generates large amount heating which makes it difficulty to distinguish the real cause of the transition.

Wu's group has demonstrated the small dose of UV light(LED) gating on VO_2[7, 95]. Their devices are made from the VO_2 nanobeam on the original grown substrate. Which makes the VO_2 has been used in their work has large embedded strain.

To further study the light effect on VO_2 single crystal nanobeam. We used strain released samples under different wavelength light. The light source used in our experiment is LED. Similar as previous reported research on stained single crystal VO_2[7, 95]. The current through the LED is controlled by Keithley 6221 DC current source. The LEDs we have tested are yellow(585nm), red(650nm), green(530nm), UV(365nm). The yellow, red and green light show no effect on the VO_2 transition. As for the UV light, the transition shifted about 1K down. The UV light used in this measurement has a power about 3.3 mW/cm^2(Estimation of UV power used in this work: The UV led has a max power of 1W, the light source and sample are spatially separated 2cm. The UV led has a view angle of 120°.). The same effect has been observed on two samples. This effect is rather different from Wu's work[7]. As shown in Wu's paper[7], around the transition, the resistance with UV and without UV shows more than two orders changes. In our device, it the resistance shows no changes with and without UV light, while the position of transition shifted about 1.5K. One explanation is the VO_2 studied in Wu's work[7] has been embedded in SiO_2 substrate. When shining UV

light, the UV light helps to soften the SiO_2 which partially release some strain.

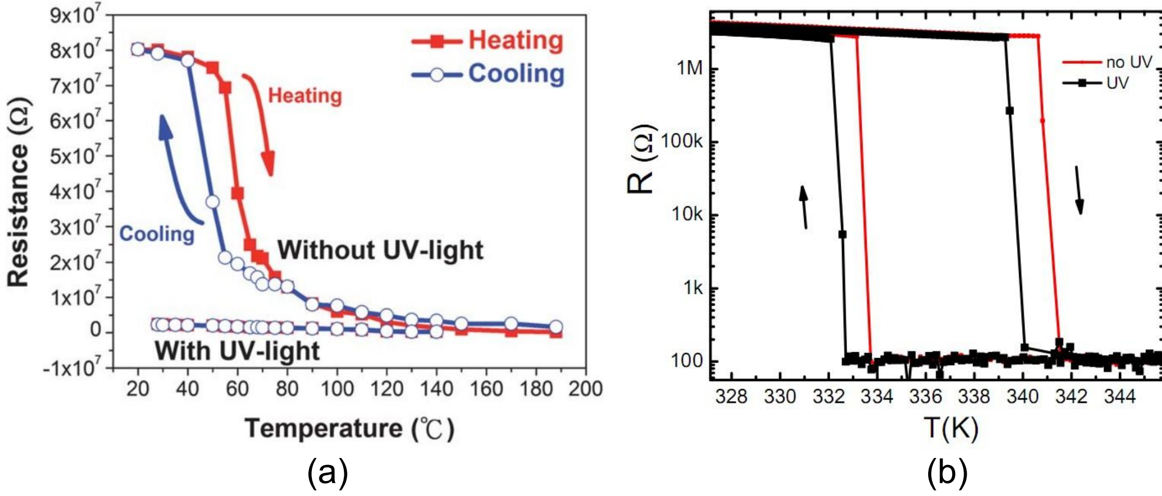

Figure 5.5: UV light effects on VO_2 transition. Left figure shows the strained VO_2 single crystal nanobeam have transition with and without UV light[7]. Right figure shows the similar condition as left when the strain is released

5.5 Capacitance on VO_2 single crystal nanobeam

5.5.1 Challenges

Compared with Polycrystalline VO_2, VO_2 nanobeam has much less effective area as a capacitor. Figure 5.6 is an image of a working device. The area of the device is less than 26μm^2. As an estimate, the geometric capacitance is:

$$C = \frac{\epsilon_0 A}{d} = 8.85\ 10^{-12} \frac{2 \times 10^{-6} \times 20 \times 10^{-6}}{30 \times 10^{-9}} F = 9.44 \times 10^{-15} F \tag{5.1}$$

Since quantum capacitance are normally larger than the geometric capacitance[4, 31, 85]. The geometric capacitance gives us an estimation of the expected level of capacitance we need to resolve. From Equation 5.1. This is on an order of 10fF. With such an small estimated capacitance to measure, the difficulty comes from a few aspects: Firstly, inside a general length BNC cable, the capacitance between the center pin and its grounding shell is ∼pF

level. The larger impedance on sample can easily force a signal goes from center pin of BNC cable to ground through the grounding shell instead through sample. Second, the substrate is 300nm SiO_2 on top of doped Si. The doped Si can form an capacitor with contact and top gate. These two capacitor then add in series to each other. The capacitance between contact and top gate and in parallel to sample capacitance. The last challenging is when using a balancing bridge to perform the measurement. The instrument which measures the balancing point will introduce another impedance which is normally smaller than sample impedance at operation frequency range.

To resolve the resolve the first challenge, we balanced at each temperature point. This makes balance point always stays at 0V relative to ground. This way, there is no potential difference across the BNC center pin and shell. To eliminate the affection from substrate, the doping layer can be grounded. This way, the contact-substrate capacitor and gate-substrate capacitor are well shield to each other. Lastly, to monitor the balance point state without introducing a smaller impedance instrument. We applied a current preamp instead of a voltage preamp in polycrystalline VO_2 capacitance measurement. The current preamp will drive the balance point to a virtual ground. Then there won't be any drop of voltage on the measuring instrument.

5.5.2 Result

Figure 5.7 focus on measurement at frequency 523Hz. The sample capacitance jumps up $\sim$0.4% at 340K. As mentioned in Chapter 1, at high temperature, the VO_2 is 1% shorter than low temperature. Since these two changes are in opposite directions, this helps us to eliminate crystal structure change as a cause. Although the capacitance jumps happens about the sample temperature as the resistivity transition, resistivity transition is not effect-

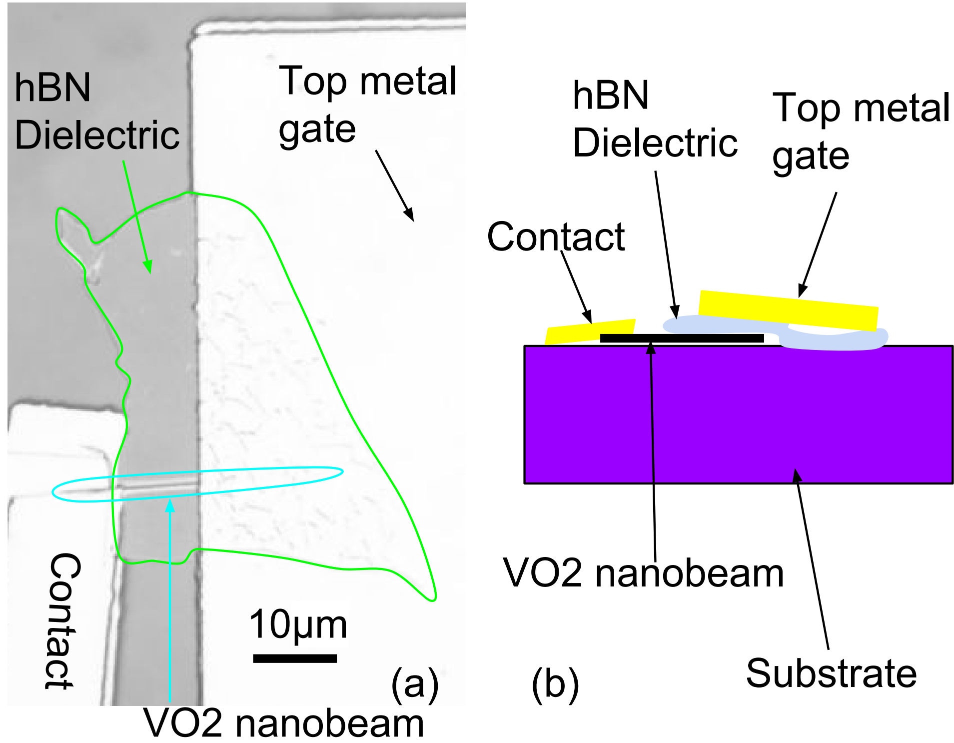

Figure 5.6: (a) Optical image of single crystal VO_2 capacitor device. The dielectric is multilayer hBN, the VO_2 nanobeam and top gate form an capacitor. The thickness of hBN is around 30nm. The length of VO_2 nanobeam underneath hBN is about 20μm. (b) Schematic of side view of the same device.

ing our observation. The resistance of VO_2 ranges from 2∼10 MΩ depends on the length. The capacitive impedance $X_C = 1/2\pi fC$ is about 24 GΩ in Figure 5.7(at 523Hz). The total resistance is less than 0.05% of capacitive impedance in the sample. Compared with capacitance measurement on polycrystalline VO_2, it is not possible to figure out an accurate effective area. Except the difficulty to measure the width of the sample, the capacitance formed is between a rod and a metal plate rather than two parallel plates. This hinders us to obtain the exact value of $dn/d\mu$ in a standard unit of $\mathrm{eV^{-1}cm^{-2}}$ or $d\mu/dn$ in unit of $\mathrm{eVcm^2}$. However, it still shows us the trend at transition in an arbitrary unit. In polycrystalline VO_2, it takes >5K for the DOS to increase from almost zero to very large. In Figure 5.7 b, C_q indicates a sudden jump of DOS at 340K. The jump is so rapid that there is no

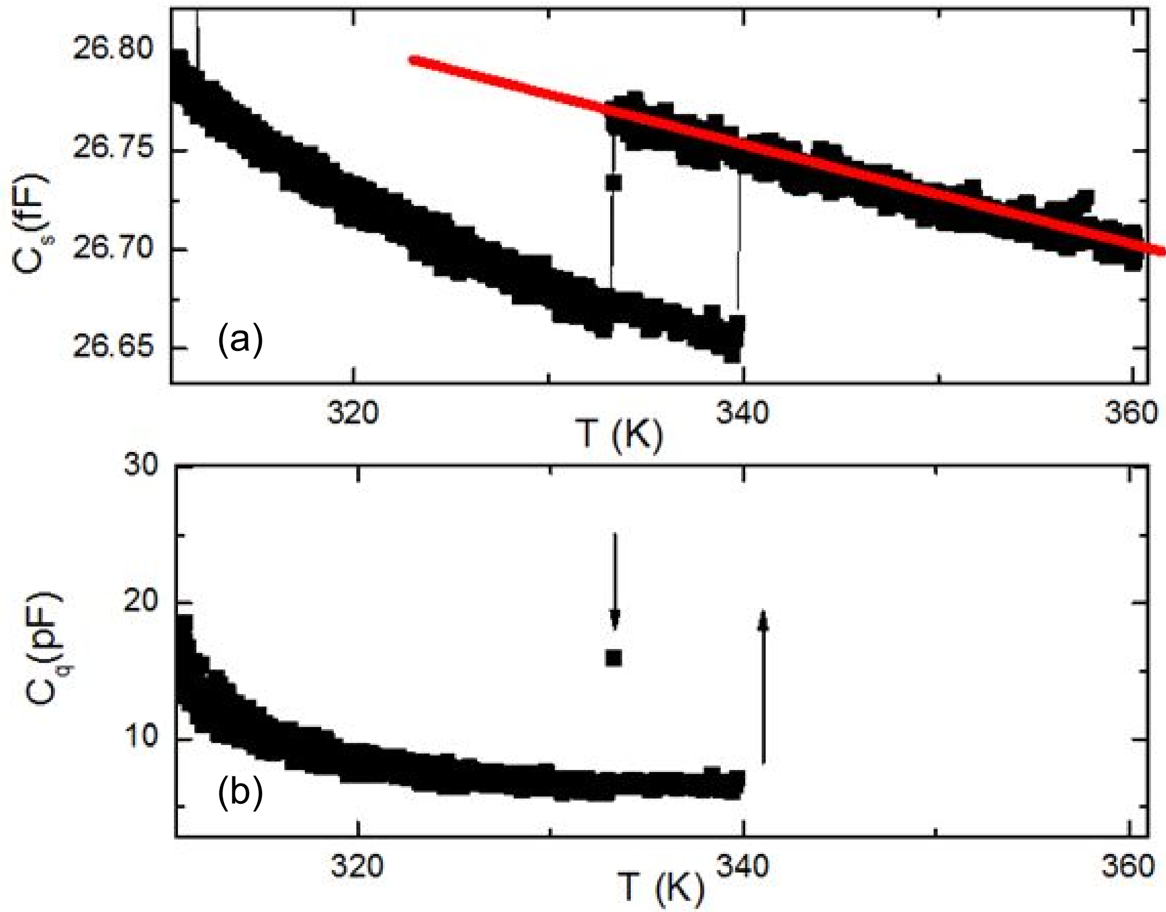

Figure 5.7: (a) Sample capacitance(black line) and fitted geometric capacitance(red line) as a function of temperature.(b) Quantum capacitance C_q.

data point is taken between two states.

However the result above still may suffer from the strain since the VO_2 used here is underneath hBN layer and metal gate. To verify our result, we have been working on another design to make the hBN as a gate underneath VO_2(see Figure 5.8). In this design, the capacitor is formed between VO_2 and its bottom metal gate, this way the strain are supposed to be significantly reduced. Note the VO_2 is made longer than the bottom metal gate width to guarantee after MIT transition the geometric capacitance is not effected due to shrink of sample. Due to technical difficulties, we haven't yet achieve an working device

in this setup.

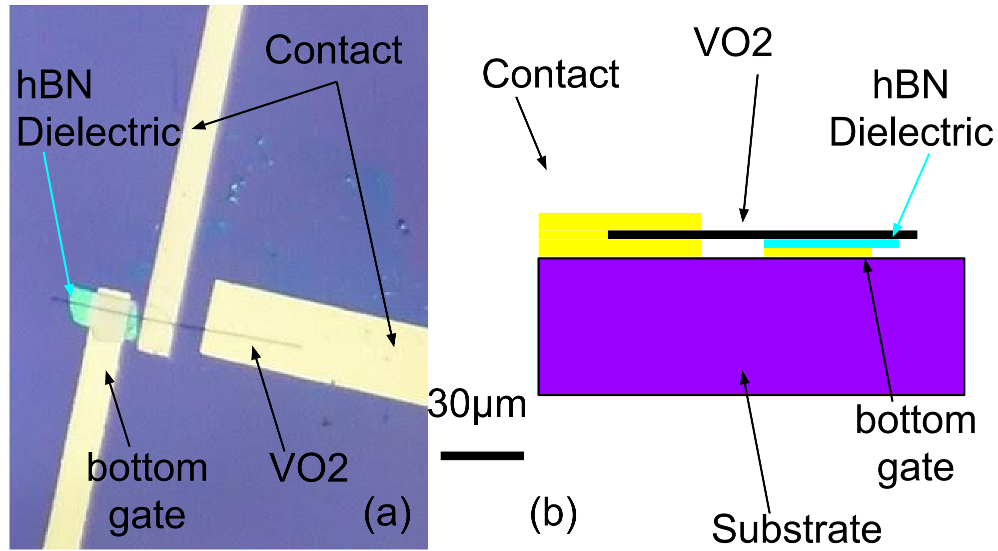

Figure 5.8: (a) Optical image of single crystal VO_2 capacitor bottom gate device. This is an unfinished device, another layer of deposition need to be done on the contacts area. (b) Schematic of side view of the same device.

CHAPTER 6 Study on GaAs HIGFET

In chapter 7, p-doped GaAs is discussed. As mentioned, one drawback of using doped GaAs system is doping may introduce disorders into system. Although delta doping can significantly increase carrier mobility by suppressing the disorder[99], the sacrifice of quality is unavoidable. The disorders caused by doping could trigger Anderson localization[51] when probing interaction driven insulating behavior. To eliminate the disorder driven effect, we have to use as less disorder as possible. Hertostructure insulating gated field effect transistor(HIGFET) is ideal for this purpose. There is no artificial doping in HIGFET, the 2D quantum well is better protected. The charge carrier is introduced from the contacts by field effect(gating).

By applying positive or negative voltage on the top gate, the carrier can be either p type or n type. Also the contacts materials have to be different for different charge carrier types: AuBe is used for p-type contacts, AuGe is used for n-type contacts. In most of our sample, we used p-type carrier. The primary reason is holes in GaAs has a effective mass a few times larger than electron[100]. Which makes it easier to reach a larger r_s value to which can create a strongly correlated system to study.

6.1 Challenging

Although HIGFET has the advantage to study interaction driven phenomenon, it is challenging to fabricate a good working HIGFET device. The gate is made by MBE grown of a heavily doped GaAs layer on top. When we do gating, the gate area has to cover all the area of 2D layer in order to avoid the edge-bulk effect. In another words, the gate area spans as large as 2D carriers.

The challenging part comes from making Ohmic contacts without shorting to the gate.

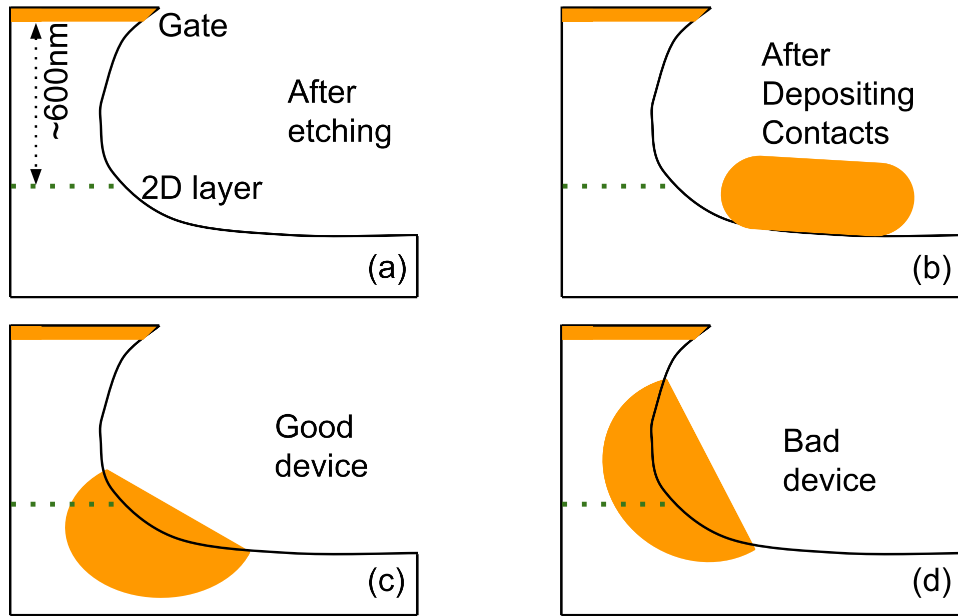

Figure 6.1: (a) The profile after etching, (b) Metal contacts deposition, (c) After annealing, metal contacts have a good Ohmic contacts with 2D layer and have a safe distance from top gate, (d) After annealing, contacts metal are too close to top gate.

As shown in Figure 6.1 a, the distance between 2D layer and gate is 600∼800nm. After deposition of metal contacts, these contacts has to be annealed to have an ohmic contact to 2D layer.

The thicker distance will increase the difficult of dark etching profile. The isotopic etching can make part of top gate breaks. With this narrow distance, we have to control the parameters to make the metal have a Ohmic to 2D layer yet keep a distance from top gate. If the distance between gate and of etching depth, deposition metal thickness, annealing temperature and time. The only way is to etch down the surface of contacts area, make the etched area a little lower than 2D carrier layer. Then deposit metal and let metal diffuse to the 2D layer. This means we have to let the contact metal material diffuse enough to have a good ohmic contacts while not too far to have a potential short to the gate. When the distance between top gate and annealed metal contacts are too short, the leakage usually don't

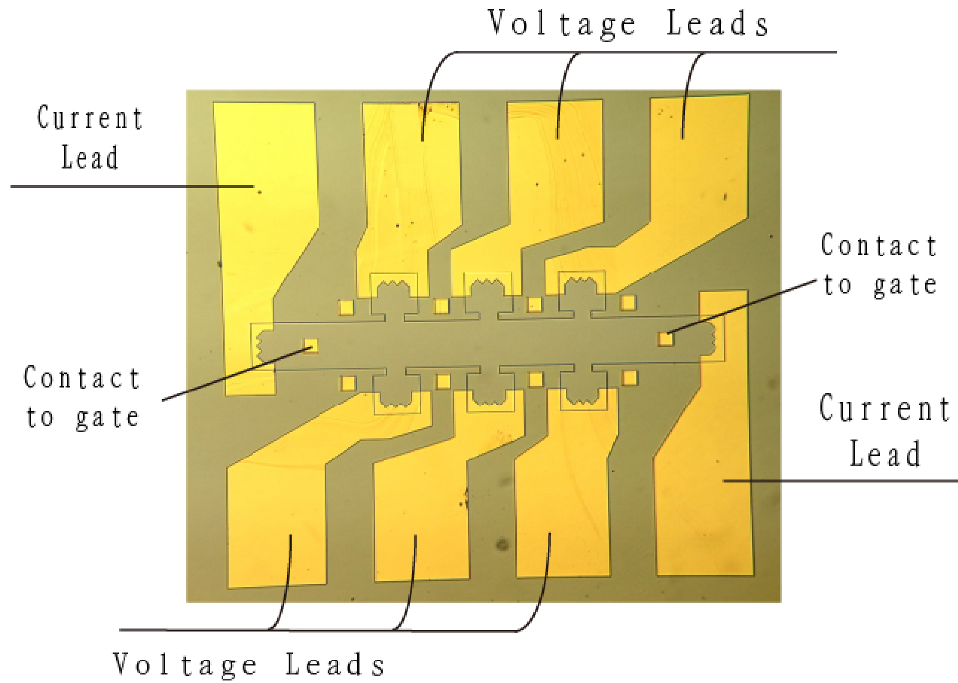

Figure 6.2: The optical image of a working HIGFET device

happen at low bias. However, to capacitively obtain large enough density, usually >1.2V is required. With this bias, the leakage can easily occur with a short distance between top gate and contacts. These make the fabrication of HIGFET rather challenging. As a matter of fact, the first working device comes after 80 trials on different parameters. Figure 6.2 shows the optical image of a working HIGFET device.

6.2 Results

The Figure 6.3 shows the turn on characteristics of a HIGFET. To protect the device, a voltage drive AC signal of 100μV is used. Prior to the device turning on, it has a huge impedance, the voltage source is essential for device protecting. The the current between drain and source I_{SD} is measured by monitoring the voltage on 1KΩ resistor in series with HIGFET.

The turn on test has been done at 5K, the result is shown in Figure 6.3. For a working

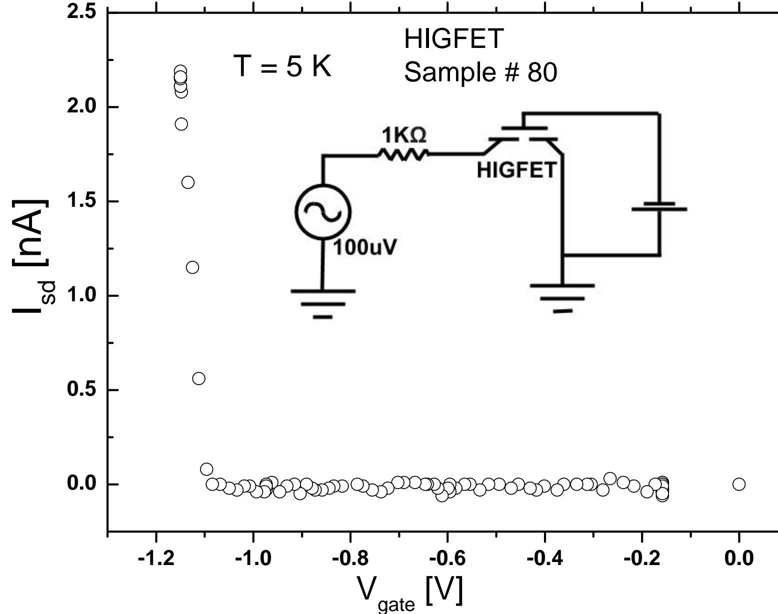

Figure 6.3: HIGFET turn on test. The inside is a schematic of testing circuit.

device, the device starts to turn on at 1.1V and fully turns on when bias is larger than 1.2V. The I_{SD} promptly jump to a few nA range when bias approaching 1.2V. For instance, when I_{SD}=2nA, the sample resistance is around a few ten KΩ.

Quantum hall effect is followed to characterize the sample at a lower temperature. As we can see from Figure 6.4, quantum hall effect has been observed under different biases. The charge carrier densities varies with tuning the gate bias. Unlike using SdH oscillation to calculate density shown in Chapter 7, HIGFET doesn't show SdH oscillation. There are two possible reasons: one is the density in HIGFET are much lower than doped sample, another reason could comes from the high temperature. The p doped sample is measured at an upgrade cooling setup which yields an lower temperature. The density is calculated from the slope of the hall resistivity using $p = \frac{1}{e}\frac{dB}{d\rho}$, and results are shown in Table 6.1. At bias 1.24V, the sample barely turns on and the hole density is 2 orders smaller than the

Gate bias(V)	$d\rho/dB(\Omega/T)$	hole density(cm^{-2})
1.24	5323800.64	1.17×10^{8}
1.3	61793.93	1.01×10^{10}
1.4	53480.88	1.18×10^{10}
1.5	35515.41	1.76×10^{10}
1.6	31155.08	2.01×10^{10}

Table 6.1: HIGFET density at different gate bias voltage

rest. The non uniformity of charge carriers at this voltage is too high which shows no hall plateau. Even at 1.3 volts, the sample shows dramatic increasing on ρ_{xx} and ρ_{Yxx}, and there is no hall plateau. The increasing on ρ_{Yxx} indicating the resistance measured are jumping out of the scope and capacitive coupling are becoming evident.

Our ultimate goal is to capture the resistivity-temperature dependence relation. This tells us whether the system is an insulating system or a conducting system. In our measurement result as shown in Figure 6.5, the plateau appeared as temperature goes lower than 100mK. This is not as expected since various density should behave differently. This observation is due to the cooling power. Although the temperature showing on the graph is measured by a precision carbon thermometer mounted on the sample stage. The sample is mounted on sample stage by gluing using silver paint. The sample it self is not cooled as well as the thermometer. At a few mK range, the electron phonon interaction is largely suppressed. The only cooling comes from the metal contacts. This is not sufficient enough.

In another words, although the Figure 6.5 shows temperature well below 100mK, the real temperature on the carrier may be much higher than that. So the plateau we see in Figure 6.5 is because the temperature is not changing on sample, but changing on thermometer.

To avoid this situation, an helium cell need to be used. The design is using a cell filled with liquid helium and sample is immersed inside the liquid helium. By doing so, we would

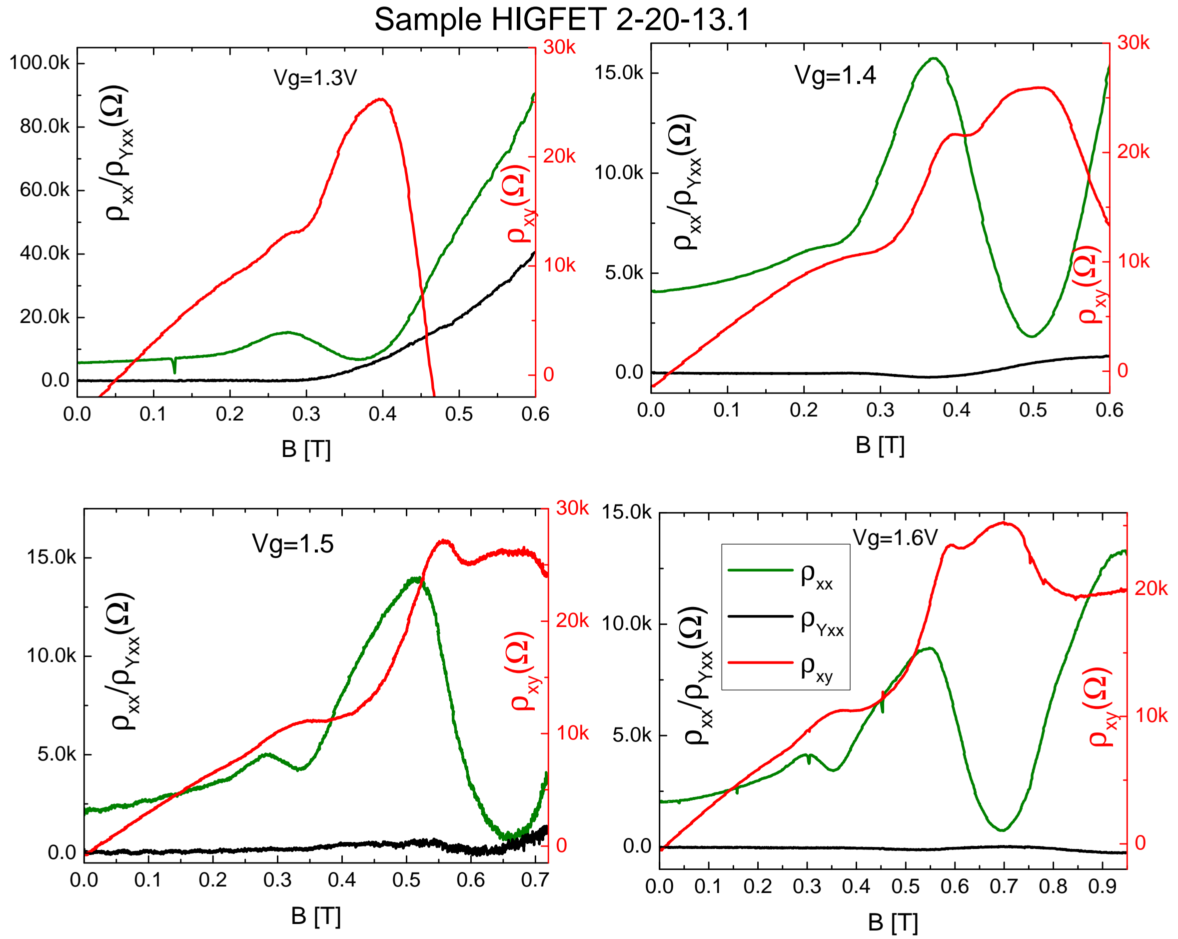

Figure 6.4: Quantum hall measurement on HIGFET

be able to maximize the cooling power on the carrier. This part we are still working on and is our future plan in probing the interaction driven state at low temperature.

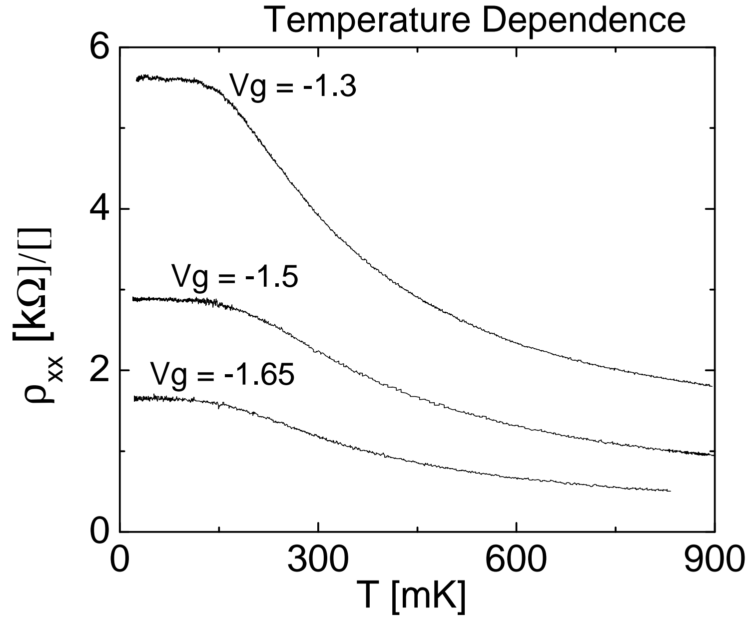

Figure 6.5: Temperature dependence on HIGFET

CHAPTER 7 Other measurement results

In this chapter, the measurement on p-doped GaAs 2D system as well as on graphene will be discussed. Part of the result of this chapter have been published in 2014[8].

7.1 p-GaAs

7.1.1 Density calculation using SdH oscillations

The sample used in this work is a two dimensional hole system. We kept stringent fabrication standard to ensure the cleanness and high quality of device. For p-doped sample, it is more plausible to deploy to study interaction driven effect. This is due to the larger effective mass of hole than electron in GaAs system. Parameter $r_s = (m^* e^2)/(4\pi\hbar^2\epsilon)(p\pi)^{-1/2}$ is generally used as an indicator for the interaction among experimental physicist. It is the ratio of the Coulomb energy and Fermi energy. When it reaches its critical value, the system can be dominated by coulomb interaction.

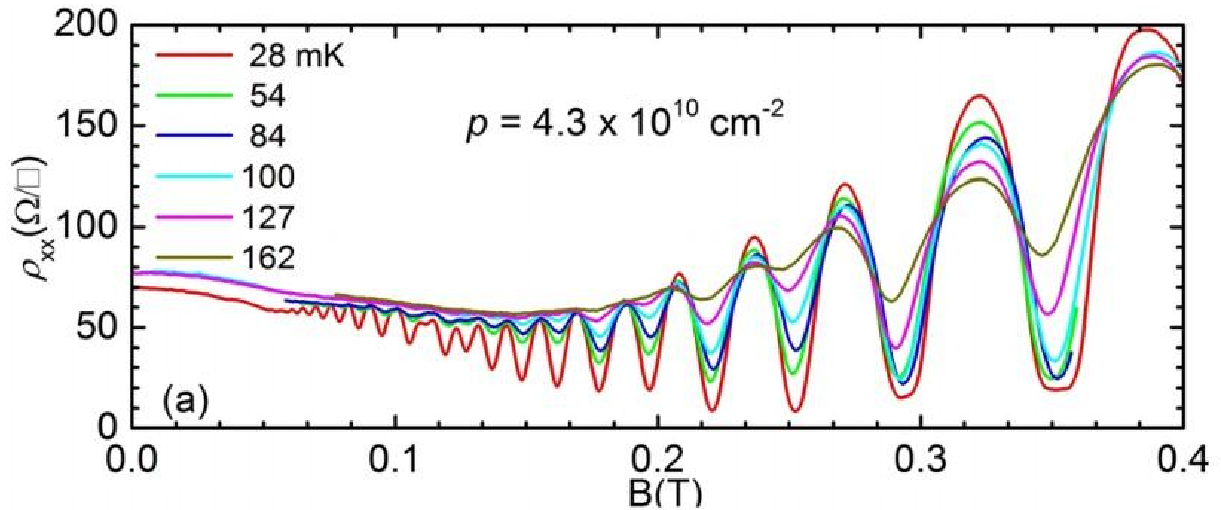

Figure 7.1: Shubnikov-de Haas (SdH) oscillations of p-doped GaAs sample[8]

Since r_s is linear to m^*, it is important for us to calculate the precision value of effective mass m^*. Figure 7.2 shows the low field Shubnikov-de Haas (SdH) oscillations. For SdH

oscillations, Figure 7.2 plot the longitudinal resistivity ρ_{xx} as a function of inverse of magnetic field(1/B). The ρ_{xx} oscillates in a period:

$$\Delta(\frac{1}{B}) = \frac{e}{h} \cdot \frac{g_s}{p} \tag{7.1}$$

In above equation: e and h are constants; g_s is spin degeneracy factor(constant=2); p stands for density in hole system. Using this equation, we can get the hole density in the system. Compared with hall effect measured density, this method can achieve a more accurate value for density.

By plotting the ρ_{xx} as a function of 1/B, we have Figure.7.2. The inset is an Fourier analysis result. As we can see, the peak is well established and lies on 0.94 T. It has been demonstrated in GaAs hole system, there exist heavy hole and light hole when the density is beyond $7{\times}10^{10}$cm^{-2}.[101]. In our sample, the density is lower than this limit[102–104]. With this, we can get the density by using Equation 7.1. The hole density obtained in our system is $4.5{\times}10^{10}$cm^{-2}[102].

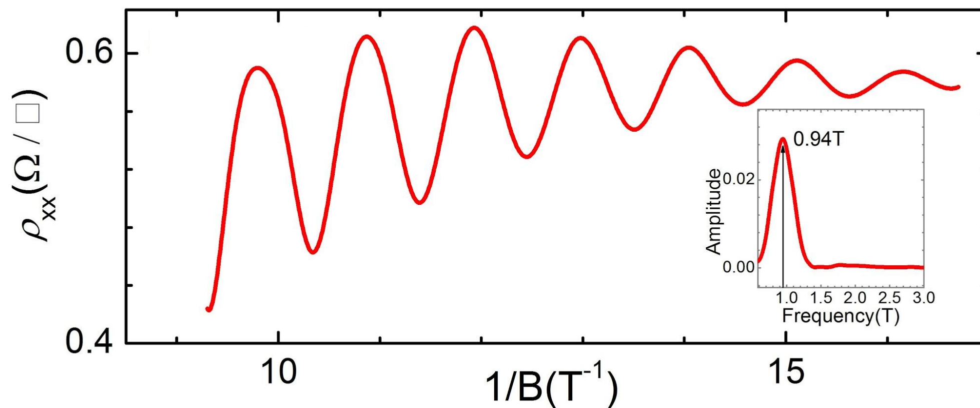

Figure 7.2: Observed SdH oscillations for the two samples, the magnetic field in the range between 8.5 T^{-1} and 15 T^{-1}. In the insets are shown the Fourier spectra of the oscillations, the dominant peaks and their frequencies values [8].

7.1.2 Effective Mass in the Valence Band of GaAs quantum well

From SdH oscillation, effective mass can also be obtained accurately[104]. In the research work Tsuneya Ando and Yasutada Uemura did in 1975[105], they explicitly illustrated how the relate effective mass with longitudinal resistivity:

$$\rho_{xx}(B) = \rho_{xx}(0)\left[1 - 4\cos\left(\frac{E_F}{\hbar\omega_c}\right)\cdot D(m^*,T)\cdot E(m^*,\tau_q)\right] \tag{7.2}$$

where $\rho_{xx}(0)$ is zero field resistivity; E(m^*,τ_q)=exp($-\pi/\omega_c\tau_q$); D(m^*,T) is the Dingle factor when the B field is low D(m^*,T)=$\xi/\sinh\xi$ with ξ=$2\pi^2$k$_B$T/$\hbar\omega_c$ [106]. In the temperature region that we are exploring, we can use the approximation for which $\ln(\sinh\xi) \sim \xi$, This can helps us to simplify Equation.(7.2). Now, m^* can be extrapolated from :

$$\ln\left(\frac{\Delta\rho_{xx}}{T}\right) = C - \frac{2\pi^2 k_B}{\hbar e B} m^* T \tag{7.3}$$

The data are fitted into the Equation.7.2. The residual square R^2 >0.995

The fitted m^* are shown in Figure.7.4. For the two sample in our measurement, m^* slightly changes with density. In the density we are considering, the Hartree potential(e-e repulsion) does not have a significant contribution to the Hamiltonian. With this consideration, the dependence of m^* on p is caused by the position of Fermi energy of 2DHS[103].

7.1.3 Anti-Hall bar bulk break down result

The Anti-Hall bar fabrication has been mentioned briefly in chapter 2. The reason it is named as Anti-Hall bar is that, compare with Hall bar, Anti-Hall bar has two edges. Which creates two topologically separated edge states. Anti-Hall bar is similar to Corbino-disk geometry, with more contacts enables characterizing sample with quantum hall effect. In

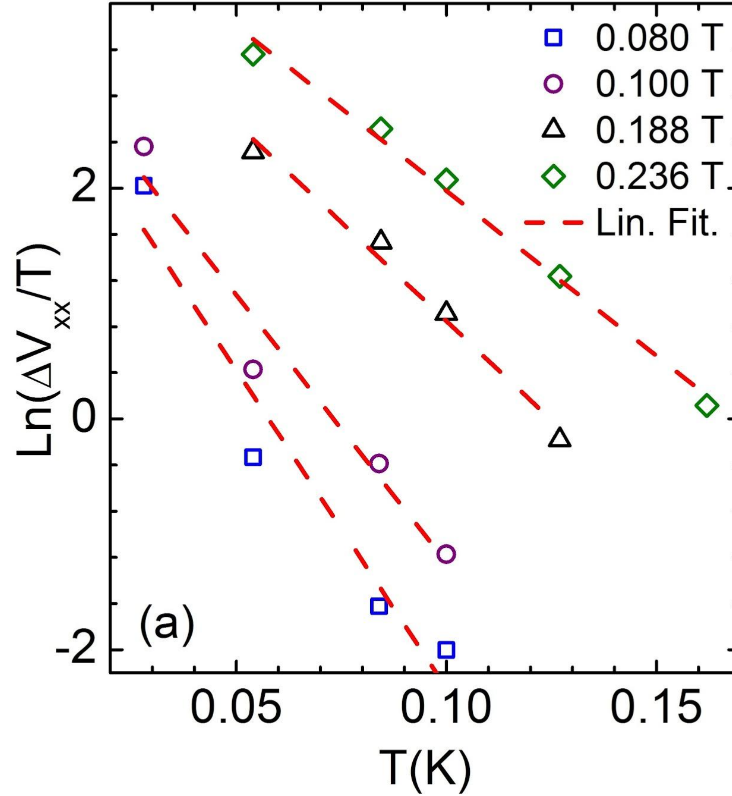

Figure 7.3: Variation of the logarithm of the longitudinal resistance with the temperature and its fit with the Dingle factor for different magnetic fields for respectively[8]

Figure 7.5(j), a DC signal and AC signal is added together and applied between the inner edge and outter edge. The magnetic field is held at 2T where integer quantum hall state ν=1 is reached. Note the choice of inner contact and outer contact doesn't change the result since all the same edge contacts are equal potential. As shown in Figure 7.5(e), at ν=1, the DC voltage needed to break down the insulating bulk is as large as 10mV. When the system is deviated from ν=1, the break down becomes easier and easier. At ν=0.92 in Figure 7.5(i), it becomes almost conducting through all the DC bias with a little bump at 0V DC bias. This system provides us an unique opportunity to probe the break down between topologically isolated states in two dimensions. It turns out that tunneling resonant contributes the break down mechanism which is discussed in more details in Refs. [43]

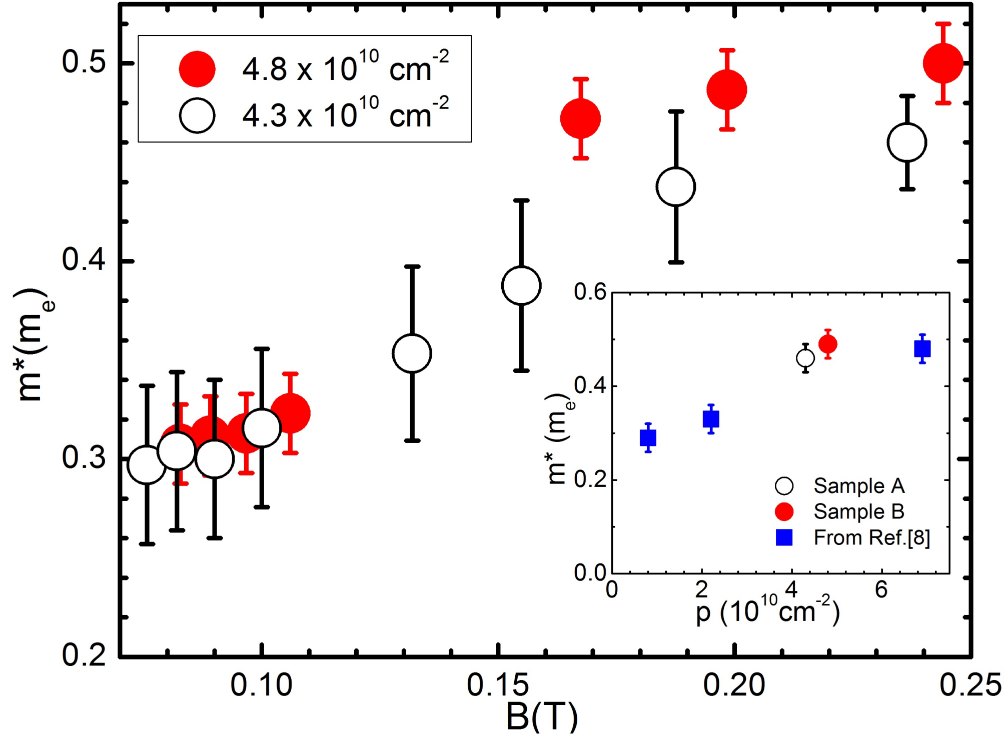

Figure 7.4: Effective mass fitted at different magnetic field strength[8], sample B is a similar sample with density p=4.9×10^{10}cm^{-2}, Inset shows our result compared to previous data obtained through cyclotron resonance measurements [9]

7.2 Graphene result

A natural graphene has been fabricated with a terminal on it. Dirac point slightly changes from 3.7V to 4V from room temperature to 4K. The quantum hall measurement performed on graphene is on fixed magnetic field(7T in Figure 7.6 a) and sweeping the gate bias. When we do the quantum hall effect on GaAs, the electrons are in Landau level: $E_n = \hbar\omega_c(n + \frac{1}{2})$. Cyclotron frequency is decided by magnetic field: $\omega_c = \frac{Be}{mc}$. Sweeping magnetic field changes the Landau level spacing, so the a contact Fermi level can go through each Landau levels. In graphene, with a fixed magnetic field at 7T, the Landau level spacing is fixed. By changing the top gate, we tune the density in graphene, which changes the Fermi level.

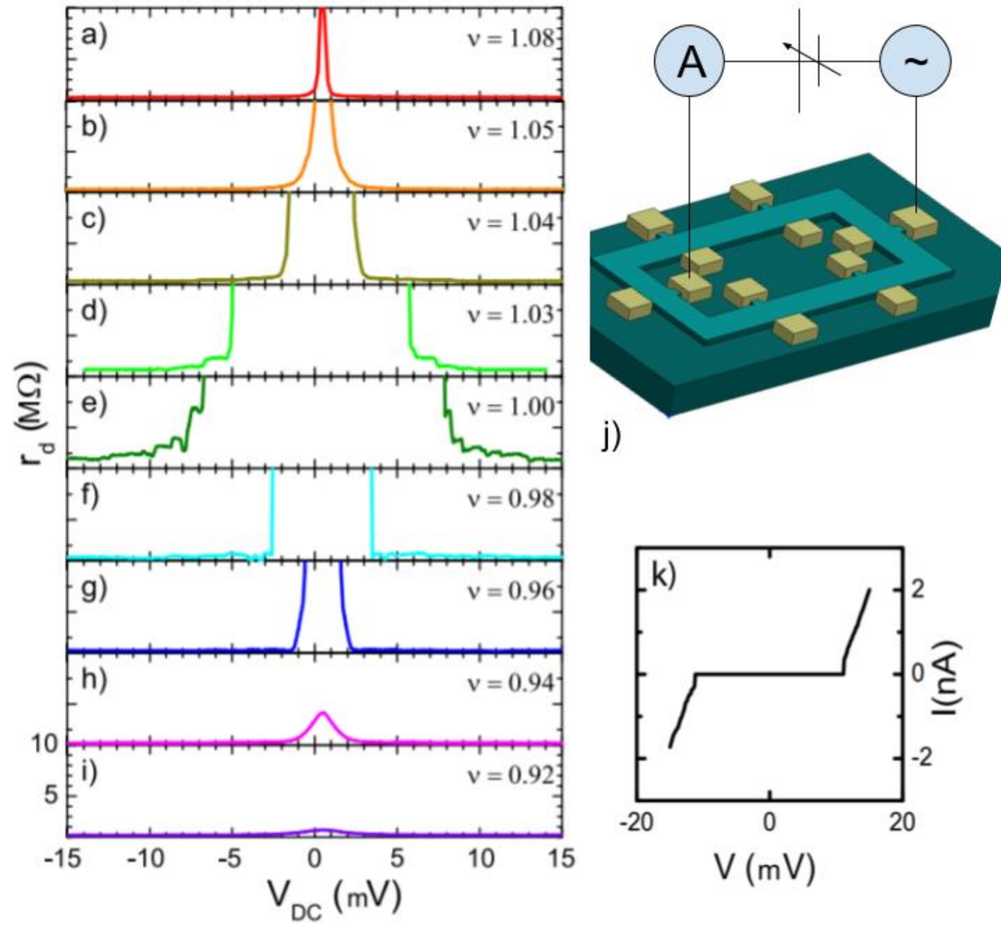

Figure 7.5: (a)-(i) Differential resistance with variours filling factors, (j) Experimental setup for measuring the bulk conduction properties with separated edges (k) I-V curve from DC measurement at $\nu = 1$

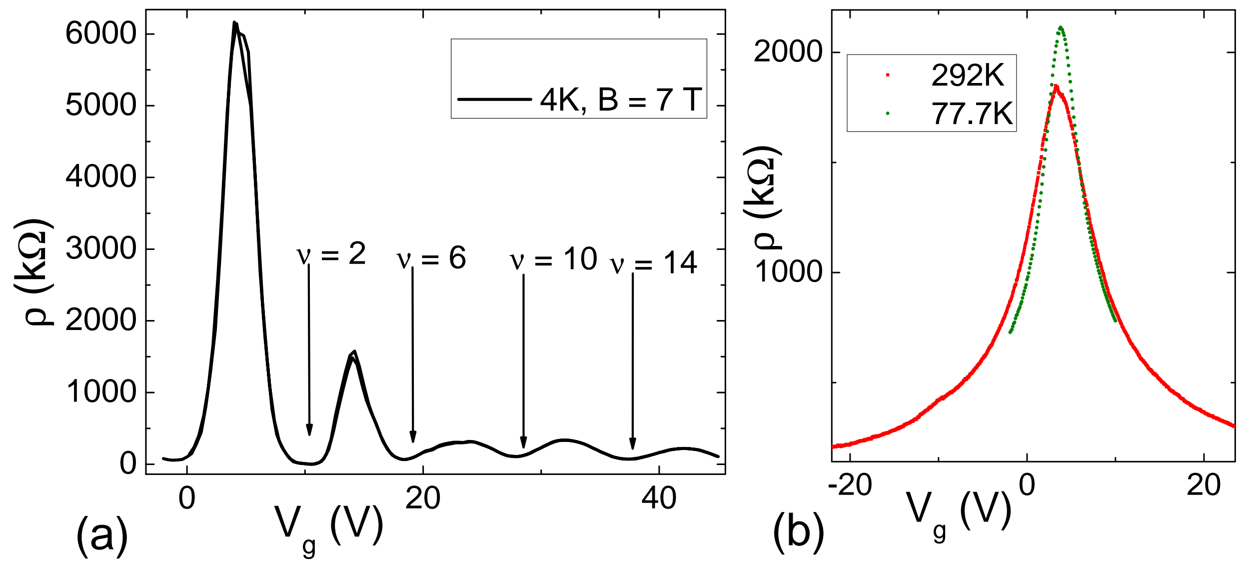

Figure 7.6: a) Quantum hall measurement on ρ_{xx}. b) Dirac point at 77.7K and 292K.

CHAPTER 8 Summary and future plan

8.1 Summary

In our research we have successfully demonstrated quantum capacitance measurement on two dimensional as well as one dimensional VO_2 system. Quantum capacitance measurements resolves $d\mu/dn$ in the system, which indicates the density of states changes trends during the transition. Lithography is the foundation to fabricate a functional electronic device. High resolution capacitance bridge enables us to probe the small change in capacitance at an extremely low excitation level. By carefully choosing the right measuring parameter, we successfully extracted quantum capacitance from the system. Our work has indicates tremendous suppress of $dn/d\mu$ on VO_2 when lowering the temperature. This agrees well with a band-gap opening at low temperature. Electronic compressibility also indicates a strongly correlation effects at lower temperature.

The Shubnikov de Haas oscillations of p-GaAs dilute 2DHS have been observed. The analysis shows the system with a density p =4.3- 4.8×10^{10}cm^{-2}. Effective mass of hole in system has also been studied by measuring the SdH oscillations-temperature dependence. The results yield 0.30-0.50 m_e when magnetic field is range from 0.08 to 0.250 T. These results are important to study strongly interacting systems when coloumb repulsion becomes significant.

8.2 Future plan

The single VO_2 capacitance measurement have been done is using hBN covered VO_2. This may cause an external strain which effect our result. To verified whether the strain cause an effect, a bottom gate sample need to be measured where gate is underneath VO_2. Only by doing so, we can eliminate the strain effect. In the mean time, the bridge resolution

at low frequency needs to be improved. We have done work in making femto Fara reference capacitance which can help to reach a balance.

The HIGFET measurement is incomplete due to the instrument repayment and upgrade. The future plan on HIGFET system includes probing lower temperature dependant behavior. The other part is applying quantum capacitance measurement on HIGFET. This method are potentially able to illustrate details on electron interactions.

BIBLIOGRAPHY

[1] J. Trail, http://sciencepole.com/wigner-crystal/.

[2] D. G. Schlom and L. N. Pfeiffer, Nature materials **9**, 881 (2010).

[3] R. Willett et al., Physical Review Letters **59**, 1776 (1987).

[4] Z. Wu et al., Applied Physics Letters **107**, 104101 (2015).

[5] B. S. Guiton, Q. Gu, A. L. Prieto, M. S. Gudiksen, and H. Park, JACS **127**, 498 (2005).

[6] CaoJ et al., Nat Nano **4**, 732 (2009), 10.1038/nnano.2009.266.

[7] J. M. Wu and L. B. Liou, Journal of Materials Chemistry **21**, 5499 (2011).

[8] V. Tarquini et al., Applied Physics Letters **104**, 092102 (2014).

[9] T. Lu et al., Applied Physics Letters **92**, 12109 (2008).

[10] F. Morin, Physical Review Letters **3**, 34 (1959).

[11] N. F. Mott and L. Friedman, Philosophical Magazine **30**, 389 (1974).

[12] H. W. Verleur, A. Barker Jr, and C. Berglund, Physical Review **172**, 788 (1968).

[13] S. Chen et al., Optical and quantum electronics **35**, 1351 (2003).

[14] F. C. Case, Journal of Vacuum Science & Technology A **2**, 1509 (1984).

[15] F. Beteille and J. Livage, Journal of Sol-Gel Science and Technology **13**, 915 (1998).

[16] A. M. Jones, D. C. Poole, B. Grassi, and P. M. Christensen, (2010).

[17] H.-T. Kim et al., New Journal of Physics **6**, 52 (2004).

[18] G. Petrov, V. Yakovlev, and J. Squier, Applied Physics Letters **81**, 1023 (2002).

[19] P. Kuiper et al., Physical Review Letters **62**, 221 (1989).

[20] J. Laverock et al., Physical Review B **86**, 195124 (2012).

[21] X. Tan et al., Scientific reports **2**, 466 (2012).

[22] C. Neuman et al., The Journal of Chemical Physics **41**, 1591 (1964).

[23] T. Yao et al., Physical review letters **105**, 226405 (2010).

[24] A. Cavalleri et al., Physical review letters **87**, 237401 (2001).

[25] Z. Tao et al., Physical review letters **109**, 166406 (2012).

[26] D. Ruzmetov et al., Physical Review B **79**, 153107 (2009).

[27] T. Yamin, Y. M. Strelniker, and A. Sharoni, Scientific reports **6** (2016).

[28] D. Ruzmetov et al., Journal of Applied Physics **107**, 114516 (2010).

[29] Z. Yang et al., Physical Review B **82**, 205101 (2010).

[30] H. Ji, PhD thesis, RICE UNIVERSITY, 2015.

[31] S. Luryi, Applied Physics Letters **52**, 501 (1988).

[32] R. Ashoori et al., Physical review letters **68**, 3088 (1992).

[33] S. V. Kravchenko et al., Phys. Rev. B **50**, 8039 (1994).

[34] S. V. Kravchenko and M. P. Sarachik, Reports on Progress in Physics **67**, 1 (2004).

[35] R. Chitra, T. Giamarchi, and P. Le Doussal, Phys. Rev. B **65**, 035312 (2001).

[36] B. Spivak et al., Rev. Mod. Phys. **82**, 1743 (2010).

[37] E. Wigner, Phys. Rev. **46**, 1002 (1934).

[38] T. Giamarchi and P. Le Doussal, Physical review letters **76**, 3408 (1996).

[39] S. Chakravarty et al., Philosophical Magazine Part B **79**, 859 (1999).

[40] R. Chitra and T. Giamarchi, J. Phys. IV France **131**, 163 (2005).

[41] J. Huang, L. N. Pfeiffer, and K. W. West, Phys. Rev. B **85**, 041304 (2012).

[42] T. Knighton et al., PhD thesis, 2017.

[43] V. Tarquini, PhD thesis, Wayne State University, 2016.

[44] G. Moore and N. Read, Nuclear Physics B **360**, 362 (1991).

[45] X. G. Wen, Phys. Rev. B **41**, 12838 (1990).

[46] X.-G. Wen, Advances in Physics **44**, 405 (1995).

[47] X.-G. Wen, International Journal of Modern Physics B **06**, 1711 (1992).

[48] Nobelprize.org, The nobel prize in physics 2016 - advanced information.

[49] C. Kittel et al., *Introduction to solid state physics*, volume 7, Wiley New York, 1996.

[50] N. W. a. Ashcroft, *Solid state physics*, 2005.

[51] P. W. Anderson, Materials Research Bulletin **8**, 153 (1973).

[52] M. Cococcioni and S. De Gironcoli, Physical Review B **71**, 035105 (2005).

[53] N. Mott, Advances in Physics **21**, 785 (1972).

[54] Y. Tokura et al., Physical review letters **70**, 2126 (1993).

[55] S. Zhang, J. Y. Chou, and L. J. Lauhon, Nano letters **9**, 4527 (2009).

[56] N. F. Mott, *Metal insulator transition*, Taylor and Francis, 1990.

[57] C. Grimes and G. Adams, Physical Review Letters **42**, 795 (1979).

[58] D. M. Ceperley and B. Alder, Physical Review Letters **45**, 566 (1980).

[59] G. Ortiz, M. Harris, and P. Ballone, Physical review letters **82**, 5317 (1999).

[60] F. Gervais and W. Kress, Physical Review B **31**, 4809 (1985).

[61] J. Wu et al., Nano letters **6**, 2313 (2006).

[62] J. Wei, Z. Wang, W. Chen, and D. H. Cobden, Nature nanotechnology **4**, 420 (2009).

[63] S. Shin et al., Physical Review B **41**, 4993 (1990).

[64] J. B. Goodenough, Journal of Solid State Chemistry **3**, 490 (1971).

[65] G. Stefanovich et al., Journal of Physics: Condensed Matter **12**, 8837 (2000).

[66] J. I. Sohn et al., Nano letters **9**, 3392 (2009).

[67] K. Appavoo et al., Nano letters **12**, 780 (2012).

[68] D. Adler, Reviews of Modern Physics **40**, 714 (1968).

[69] M. M. Qazilbash et al., Science **318**, 1750 (2007).

[70] L. Pfeiffer, Nsf funding proposal, 2009.

[71] L. Zhang et al., Journal of Physics: Condensed Matter **26**, 086002 (2014).

[72] D. Goldhaber-Gordon et al., arXiv preprint cond-mat/9707311 (1997).

[73] T. S. Kulmala et al., International Society for Optics and Photonics , 942204 (2015).

[74] M. Sahana et al., Journal of Materials Chemistry **12**, 333 (2002).

[75] R. Bunshah et al., Journal of Vacuum Science & Technology A **3**, 553 (1985).

[76] D. Kim and H. S. Kwok, Applied physics letters **65**, 3188 (1994).

[77] K. Okimura and N. Kubo, Thin Solid Films **515**, 4992 (2007).

[78] B.-G. Chae et al., Electrochemical and solid-state letters **9**, C12 (2006).

[79] T. Wang et al., ACS nano **9**, 4371 (2015).

[80] J. Cao et al., Nature nanotechnology **4**, 732 (2009).

[81] M. Stone, *Quantum Hall Effect*, World Scientific, 1992.

[82] V. J. Goldman, Nature Physics **3**, 517 (2007).

[83] J. Xia, F. Chen, J. Li, and N. Tao, Nature nanotechnology **4**, 505 (2009).

[84] J. Eisenstein, L. Pfeiffer, and K. West, Physical Review Letters **68**, 674 (1992).

[85] L. Li et al., Science **332**, 825 (2011).

[86] G. D. Mahan, *Many-particle physics*, Springer Science & Business Media, 2013.

[87] A. Bard et al., Electrochemical methods second ed, 2001.

[88] F. J. Morin, Phys. Rev. Lett. **3**, 34 (1959).

[89] T. Wei et al., Applied Physics Letters **108**, 053503 (2016).

[90] S. Sengupta et al., Applied Physics Letters **99**, 062114 (2011).

[91] K. Liu et al., Nano letters **12**, 6272 (2012).

[92] J. Wei, Z. Wang, W. Chen, and D. H. Cobden, Nature Nanotechnology **4**, 420 (2009).

[93] V. Kuznetsov et al., Soviet Physics Technical Physics **28**, 993 (1983).

[94] G. Seo et al., Applied Physics Letters **100**, 011908 (2012).

[95] J. M. Wu and W. E. Chang, ACS Applied Materials & Interfaces **6**, 14286 (2014).

[96] M. Yang et al., Scientific reports **6** (2016).

[97] S. A. Dönges et al., Nano letters (2016).

[98] T. Huffman et al., Physical Review B **87**, 115121 (2013).

[99] L. Pfeiffer et al., MRS Proceedings **145**, 3 (1989).

[100] D. Broido and L. Sham, Physical Review B **31**, 888 (1985).

[101] Y. Chiu et al., Phys. Rev. B **84**, 155459 (2011).

[102] V. Tarquini et al., Applied Physics Letters **104**, 092102 (2014).

[103] T. Knighton et al., Applied Physics Letters **104**, 193109 (2014).

[104] T. Knighton et al., Physical Review B **90**, 165117 (2014).

[105] T. Ando and Y. Uemura, Journal of the Physical Society of Japan **36**, 959 (1974).

[106] R. B. Dingle, Proceedings of the Royal Society of London A **211**, 517 (1952).

ABSTRACT

QUANTUM CAPACITANCE STUDY OF NOVEL TWO- AND ONE-DIMENSIONAL SYSTEMS

by

Zhe Wu

May 2017

Advisor: Dr. Jian Huang

Major: Physics

Degree: Doctor of Philosophy

Among strongly correlated systems, vanadium dioxide(VO_2) shows metal insulator transition(MIT) near room temperature(340K). Both Mott transition and structural transition contribute to the MIT in VO_2. To gain a better understanding of the changing electronic structures, we perform quantum capacitance measurement. Quantum capacitance measurement has already yielded insight into a variety of systems, including the negative compressibility for strongly interacting charges in GaAs two-dimensional charges. Our work demonstrates a unique method to accurately distinguish the quantum capacitance from large resistance changes at the MIT by using a home-made capacitance bridge. We observe a steep increase in the density of states (DOS) near Fermi energy as the sample approaches a metallic state upon heating. Our work is the first experimental study directly to probe the DOS during the MIT in VO_2 and is important for unraveling the long-standing mystery behind the driving mechanism for this phase change. Additionally, the bridge method for measuring the quantum capacitance in a highly resistive sample can be readily applied to other systems that exhibit a MIT, which is universal to many systems.

The consequences of electron-electron interactions are far-reaching and universal to many

systems. Present research seeks to understand the role of e-e interactions and whether these can drive a strongly correlated ground state such as Wigner crystal or Wigner glass. One of the major barriers to experimental progress in this area is the difficulty of fabricating high purity samples with dilute charges. Furthermore, making Ohmic contact to dilute charge systems represents a significant challenge. A significant portion of this work is to fabricate ultra-high purity devices using both doped p-type GaAs/AlGaAs quantum square wells and un-doped heterojunction gated field effect transistors (HIGFETS). These samples demonstrate excellent mobility at low charge densities, allowing us to identify pinning behavior in the reentrant insulating phase near in the fractional quantum Hall regime and also to probe the transport between two edges of a topological insulator. These studies are critical to understanding the physics of strongly correlated charges and their relation to topological phases, which is a fascinating area of intense current research.

AUTOBIOGRAPHICAL STATEMENT

Name:

Zhe Wu

Education:
B.S. Physics, Beihang University, Beijing, China, 2011
M.S. Physics, Wayne State University, Detroit, Michigan, 2014
Professional Experience:
Graduate Teaching and Research Assistant, Dept. of Physics and Astronomy, Wayne State University, 2011-2016
Publications:
"Degeneracy and Effective Mass in the Valence Band of Two-Dimensional (100)-GaAs Quantum Well Systems", Applied Physics Letters, 2014
"Large intrinsic inductance in strongly correlated GaAs two-dimensional holes in the integer quantum hall regime", Applied Physics Letters, 2014
"Reentrant insulating phases in the integer quantum hall regime", Physical Review B, 2014
"Polycrystalline VO2 film characterization by quantum capacitance measurement", Applied Physics Letters, 2015
"Non-uniform Hall potential and step-like breakdown of the quantum Hall effect", in preparation, 2016
"Pinning of a Quantum Wigner Crystal", in preparation, 2016